U.S. Department of Energy
FreedomCAR and Vehicle Technologies, EE-2G
1000 Independence Avenue, S.W.
Washington, D.C. 20585-0121

FY 2008

INVESTIGATIONS INTO HIGH TEMPERATURE COMPONENTS AND PACKAGING

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December 2007

OAK RIDGE
NATIONAL LABORATORY
MANAGED BY UT-BATTELLE
FOR THE DEPARTMENT OF ENERGY

ORNL/TM-2007/159

Engineering Science and Technology Division

Investigations into High Temperature Components and Packaging

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Publication Date: December 2007

Prepared by the
OAK RIDGE NATIONAL LABORATORY
Oak Ridge, Tennessee 37831
managed by
UT-BATTELLE, LLC
for the
U.S. DEPARTMENT OF ENERGY
Under contract DE-AC05-00OR22725

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ACRONYMS

A	ampere
CALCE	Center for Advanced Life Cycle Engineering
DAQ	data acquisition system
dc	direct current
DF	dissipation factor
DUT	device under test
ESR	effective series resistance
FC	fuel cell
HEV	hybrid-electric vehicle
IC	internal combustion
IGBT	insulated gate bipolar transistor
IPM	intelligent power module
JFET	junction field-effect transistor
LCR	inductance, capacitance, and resistance
MOSFET	metal oxide semiconductor field-effect transistor
NETL	National Energy Technology Laboratory
ORNL	Oak Ridge National Laboratory
PEEMRC	Power Electronics and Electric Machinery Research Center
PHEV	plug-in hybrid-electric vehicle
rpm	revolutions per minute
RTOS	real-time operating system
Si	silicon
SiC	silicon carbide
SOI	silicon on insulator
UDDS	Urban Driving Scheme
WBG	wide-bandgap

This report documents activity in support of high temperature power electronics.

1.0 INTRODUCTION

The purpose of this report is to document the work that was performed at the Oak Ridge National Laboratory (ORNL) in support of the development of high temperature power electronics and components with monies remaining from the Semikron High Temperature Inverter Project managed by the National Energy Technology Laboratory (NETL).

High temperature electronic components are needed to allow inverters to operate in more extreme operating conditions as required in advanced traction drive applications. The trend to try to eliminate secondary cooling loops and utilize the internal combustion (IC) cooling system, which operates with approximately 105°C water/ethylene glycol coolant at the output of the radiator, is necessary to further reduce vehicle costs and weight. The activity documented in this report includes development and testing of high temperature components, activities in support of high temperature testing, an assessment of several component packaging methods, and how elevated operating temperatures would impact their reliability.

This report is organized with testing of new high temperature capacitors in Section 2 and testing of new 150°C junction temperature trench insulated gate bipolar transistor (IGBTs) in Section 3. Section 4 addresses some operational OPAL-GT information, which was necessary for developing module level tests. Section 5 summarizes calibration of equipment needed for the high temperature testing. Section 6 details some additional work that was funded on silicon carbide (SiC) device testing for high temperature use, and Section 7 is the complete text of a report funded from this effort summarizing packaging methods and their reliability issues for use in high temperature power electronics.

Components were tested to evaluate the performance characteristics of the component at different operating temperatures. The temperature of the component is determined by the ambient temperature (i.e., temperature surrounding the device) plus the temperature increase inside the device due the internal heat that is generated due to conduction and switching losses. Capacitors and high current switches that are reliable and meet performance specifications over an increased temperature range are necessary to realize electronics needed for hybrid-electric vehicles (HEVs), fuel cell (FC) and plug-in HEVs (PHEVs). In addition to individual component level testing, it is necessary to evaluate and perform long term module level testing to ascertain the effects of high temperature operation on power electronics.

2.0 CAPACITOR TESTING

A test sequence has been developed to test the performance capability of advanced capacitors for potential use in transportation related applications. An ESPEC environmental chamber is utilized to produce a controlled ambient temperature so that capacitor performance can be determined at various ambient temperatures. For these tests, the temperature in the environmental chamber was cycled over its temperature range in steps of 20°C. The environmental chamber has the capability to control the ambient temperature from -70–180°C.

Capacitors are tested in two modes: static and dynamic. Static mode tests are performed without power being applied to the device under test (DUT) so the temperature of the device is determined solely by the ambient conditions. Effective series resistance (ESR), dissipation factor (DF), and capacitance are measured during static mode tests. The dynamic mode test requires a direct current (dc) bias voltage and ripple current to be applied to the DUT. The maximum ripple current at different ambient temperatures is determined during the dynamic mode test. DC bus capacitors used in inverters require high ripple current capability to protect the battery and insure its reliability and longevity.

Capacitor testing in the static mode requires a thermal cycling process that must continue uninterrupted for extended periods of time. To accomplish this long term testing, an automated data acquisition system (DAQ) using a LABView interface was developed to control an environmental chamber and log data from an Agilent 4284 inductance, capacitance, and resistance (LCR) meter. This system allows the operator to specify upper and lower temperature limits as well as temperature steps to be used during the evaluation. The program commands a target temperature to the environmental chamber and when that temperature has been reached, it monitors a capacitor parameter until stable. The program then logs the capacitor data from the LCR meter at predefined test frequencies before another temperature step is commanded.

Capacitor testing in the dynamic mode is accomplished in these tests by manually commanding a temperature to the environmental chamber and allowing the capacitor temperature to stabilize at that temperature before applying a ripple current. Thermocouples are attached to the capacitor during the dynamic test allowing the temperature of the capacitor to be monitored. After the temperature has stabilized, a ripple current is applied and the capacitor temperature is recorded. The ripple current is increased and the process is repeated. Ripple current values are determined by the size and type of capacitor being tested.

Testing was performed on new Murata ceramic capacitors and SBE "Power Ring" film capacitors using the ESPEC environmental test chamber in both the static and dynamic test modes. The SBE film capacitors are configured in a new geometry that shortens the resistive path from the terminals resulting in lower ESR. The reduction in the ESR leads to reduced heating within the capacitor and enables them to be operated at higher temperatures.

Figure 2.1 shows the ESPEC test chamber that was used during the tests. There is an access port on the left side of the chamber for instrumentation and power cables. The amplifier rack utilized is shown in Fig. 2.2. Additional instrumentation used during the capacitors tests is shown in Fig. 2.3.

Fig. 2.1. ESPEC environment chamber.

Fig. 2.2. Current amplifier rack.

Fig. 2.3. Instrumentation for the capacitor tests.

2.1 MURATA 25 μF CAPACITOR TESTS

2.1.1 Static Murata Tests

Static testing was performed on a Murata 25 μF 630 Vdc ceramic capacitor, shown in Fig. 2.4. The pins were removed and leads attached to allow attachment to the current source. A thermocouple was also adhered to the surface of the capacitor.

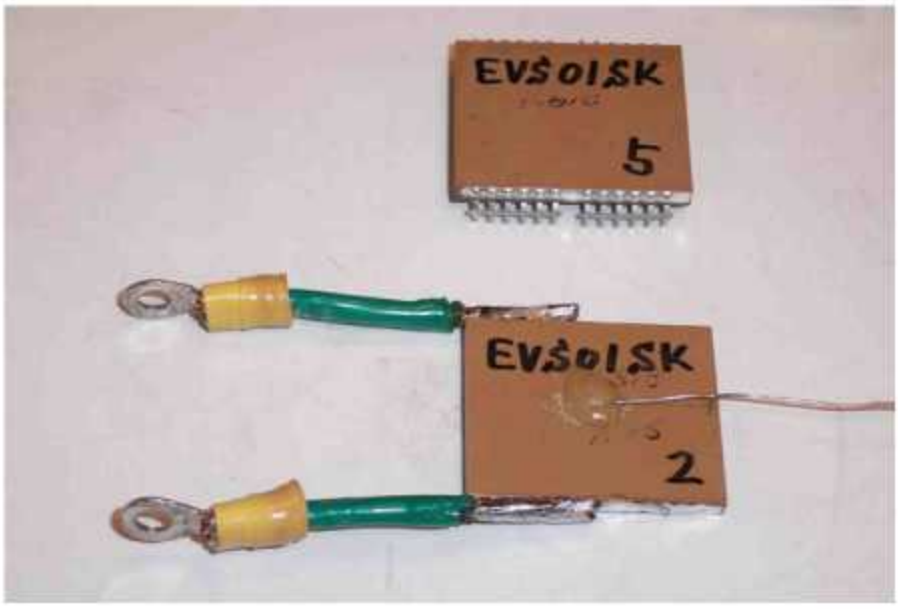


Fig. 2.4. Murata 25 μF 630 Vdc ceramic capacitor.

The Murata ceramic capacitor was tested in the static mode from 0–180°C over a frequency range of 1–40 kHz.

The graph in Fig. 2.5 shows ESR versus frequency for each temperature step.

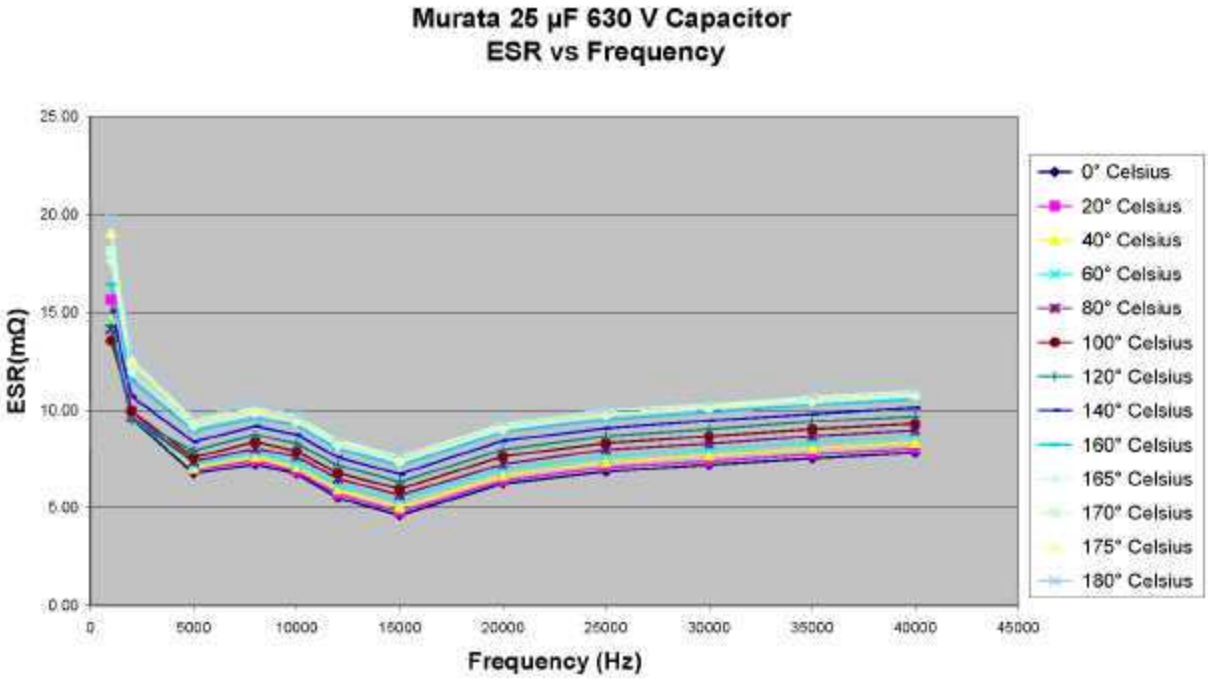


Fig. 2.5. Murata 25 µF ceramic capacitor ESR frequency response.

ESR is the sum of the in-phase ac resistances. For a given frequency, ESR increases with increasing temperatures. ESR acts like a resistor in series with a capacitor. The higher the ESR, the higher the losses in the capacitor and the more power is dissipated. If the power dissipation is too high, the capacitor heats up to a point that values change (causing drift in operation) or the capacitor fails.

During these tests, the ESR decreased 53% from 1–5 kHz at 0°C. At 180°C, the ESR decreased 51% from 1–5 kHz. The ESR increased 15% from 5–40 kHz at 0°C. At 180°C, the ESR increased 14% from 5–40 kHz.

Figure 2.6 shows the same information graphed with ESR versus temperature, illustrating fairly stable performance over temperature at a given frequency.

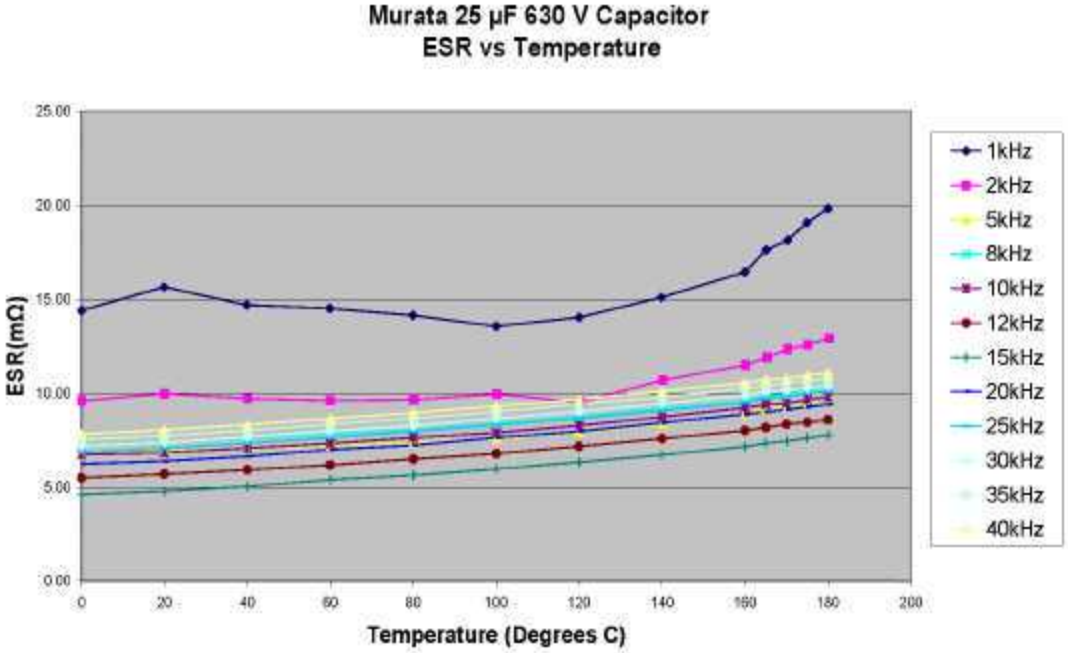


Fig. 2.6. Murata 25µF capacitor—ESR vs. temperature from 0–180°C.

Figure 2.7 shows the capacitance variation over the frequency range of 1–40 kHz at each temperature step.

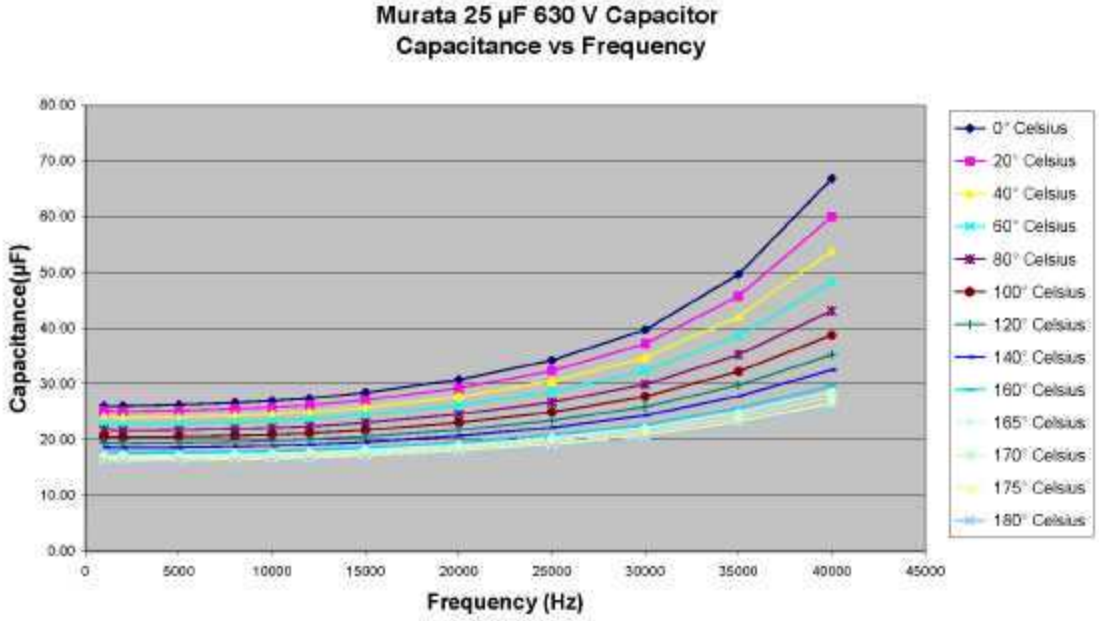
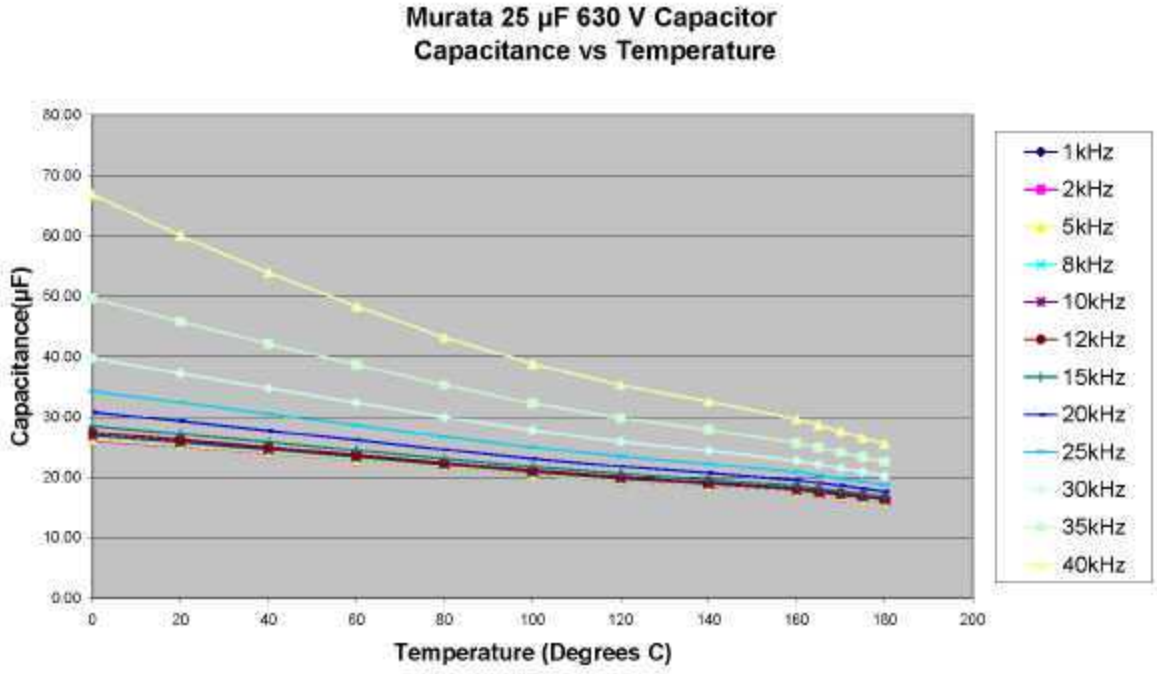


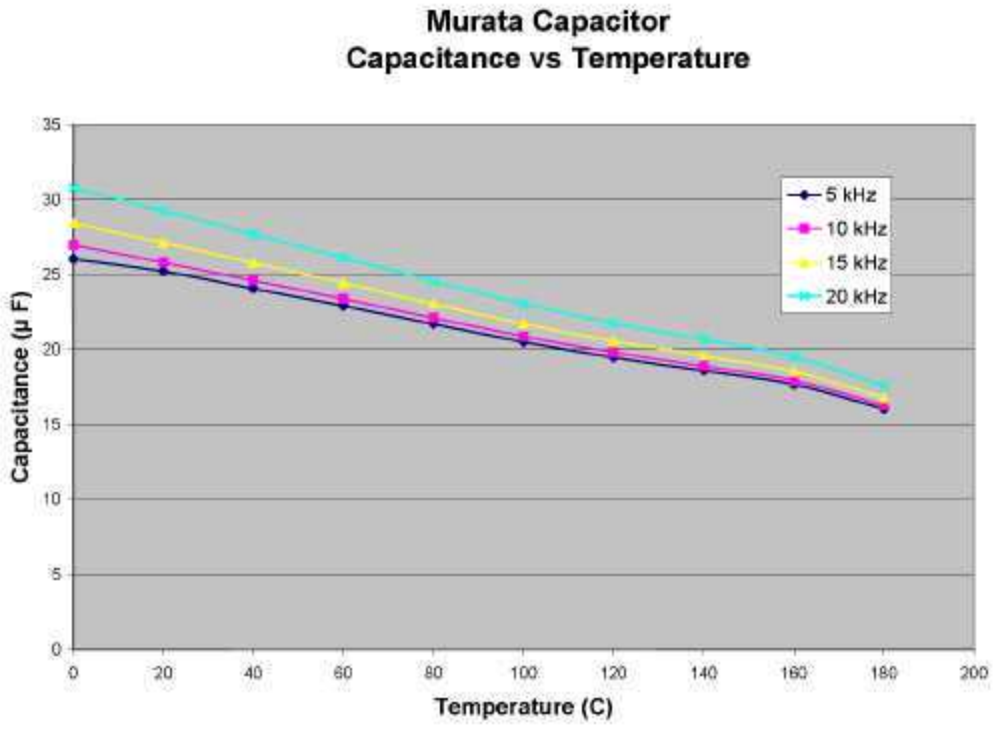
Fig. 2.7. Murata 25 µF ceramic capacitor frequency response

The capacitance increased 157% from 1–40 kHz at 0°C. Above 15 kHz the increase was 147%. Between 1–15 kHz, the capacitance value increased only 10% at 0°C. At 180°C, the capacitance increased 60% from 1–40 kHz. Above 15 kHz, the increase in capacitance was 51% at 180°C. Between 1–15 kHz, the capacitance increased by 9% at 180°C.

Figure 2.8 graphs the capacitance variation over temperature at different frequencies.



(a)



(b)

Fig. 2.8. (a) Murata 25 µF capacitor—capacitance vs. temperature, and (b) Murata 25 µF capacitor—capacitance vs. temperature.

Changing the y-axis scaling and selecting a few frequencies of interest, it can be seen from Fig. 2.8(b) that a significant decrease in capacitance occurs over temperature from 0–180°C.

Figure 2.9 shows the DF over the frequency range of 1–40 kHz at each temperature step.

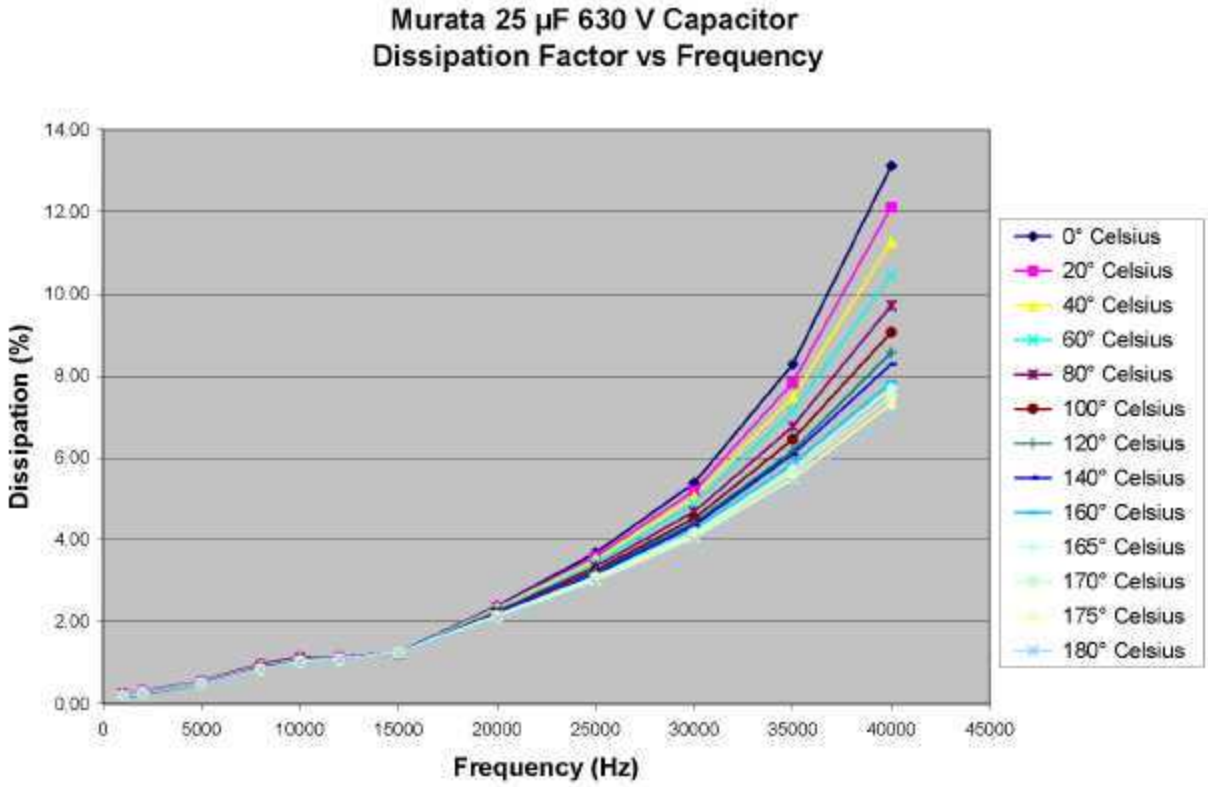


Fig. 2.9. Murata 25 µF ceramic capacitor DF vs. frequency.

The DF is the ratio of power loss in the capacitor to the total power transmitted through the capacitor. The DF is a ratio of a capacitor's resistance (ESR) to its capacitive reactance (Xc). DF is usually expressed as a percentage (i.e., ESR/Xc * 100%). A capacitive reactance (Xc) is calculated by the expression $Xc = 1/(2\pi fC)$. The DF increases with increasing frequency. At a given frequency, the DF shows some decrease with increasing temperature.

The Murata 25 µF ceramic capacitor has a .2% DF at 1 kHz and 180°C. This changed to 1.23% DF at 15 kHz and 180°C, which is a 515% increase. At 0°C and 1 kHz, the DF is .23% and increases to 1.24% at 15 kHz and 0°C, which is a 439% increase.

Between 15 kHz and 40 kHz at 180°C, the DF increases 469% and between 15 kHz and 40 kHz at 0°C, the DF increases 948%.

Figure 2.10 graphs the DF versus temperature showing fairly stable values for the lower frequencies tested.

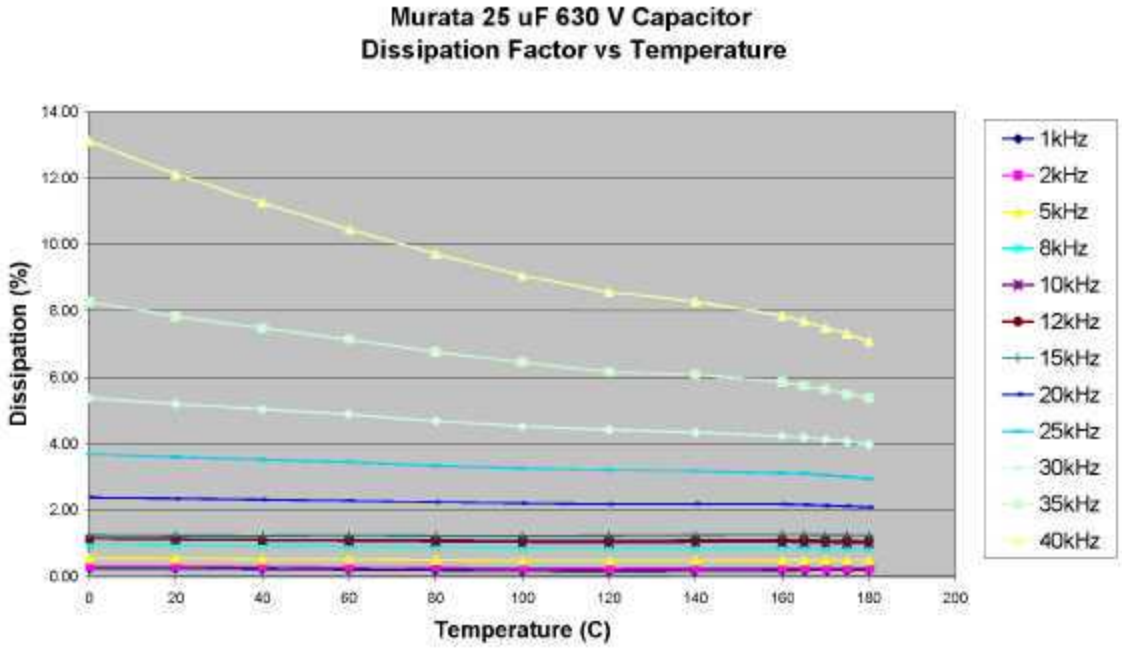


Fig. 2.10. Murata 25 µF capacitor—DF vs. temperature.

2.1.2 Dynamic Murata Tests

The Murata 25 µF 630 Vdc ceramic capacitor was tested in the dynamic mode. Figure 2.11 shows the temperature rise relative to ripple current values.

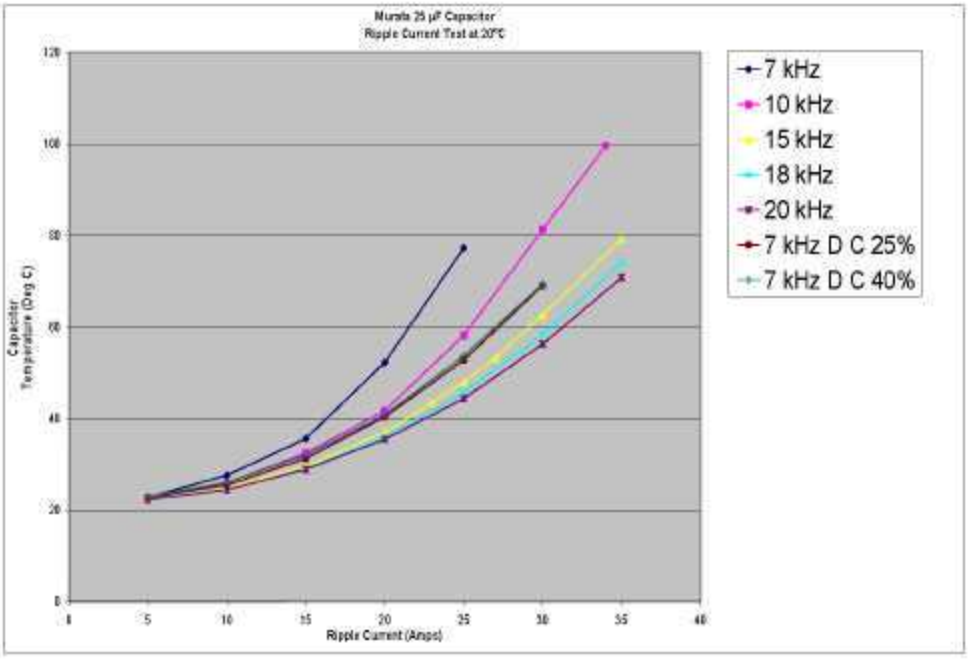


Fig. 2.11. Murata 25 µF ripple current at multiple frequencies.

The ripple current tests were not intended to be a test to failure, only to get an indication of how the capacitor responded to ripple current at various frequencies. Ripple current at higher frequencies generated a lower temperature rise than ripple current at lower frequencies.

At 20 kHz with an ambient temperature of 20°C, 25 A of ripple current generated a temperature of 44.4°C on the surface of the capacitor. At 7 kHz with an ambient temperature of 20°C, 25 A of ripple current resulted in a temperature of 77.3°C on the surface of the capacitor.

2.2 SBE 580 µF CAPACITOR TESTS

2.2.1 Static SBE Tests

Static testing was performed on a SBE 580 µF 100 Vdc power ring film capacitor, shown in Figs. 2.12 and 2.13. This capacitor's geometry is structured to enable significantly more heat transfer by shortening the distance of the current flow between the terminals. This novel approach lends itself to higher temperature operation in innovative inverter designs.

Fig. 2.12. SBE 580 µF 100 Vdc film capacitor.

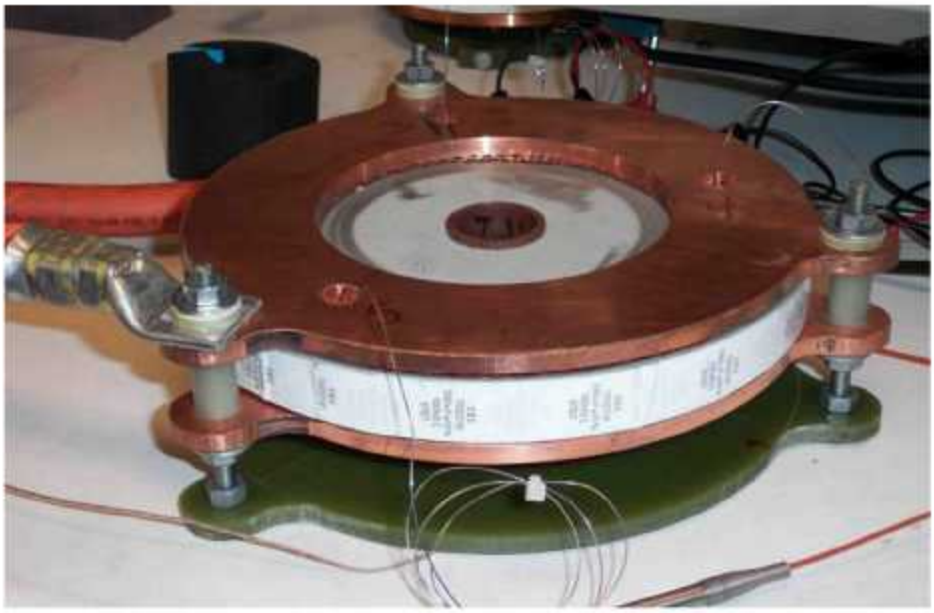


Fig. 2.13. SBE 580 µF 100 Vdc film capacitor with test fixture and thermocouples attached.

The SBE 580 µF 100 Vdc film capacitor was tested in the static mode from -40–140°C over a frequency range of 1–30 kHz. Figure 2.14 shows the variation of ESR versus frequency response at each temperature step.

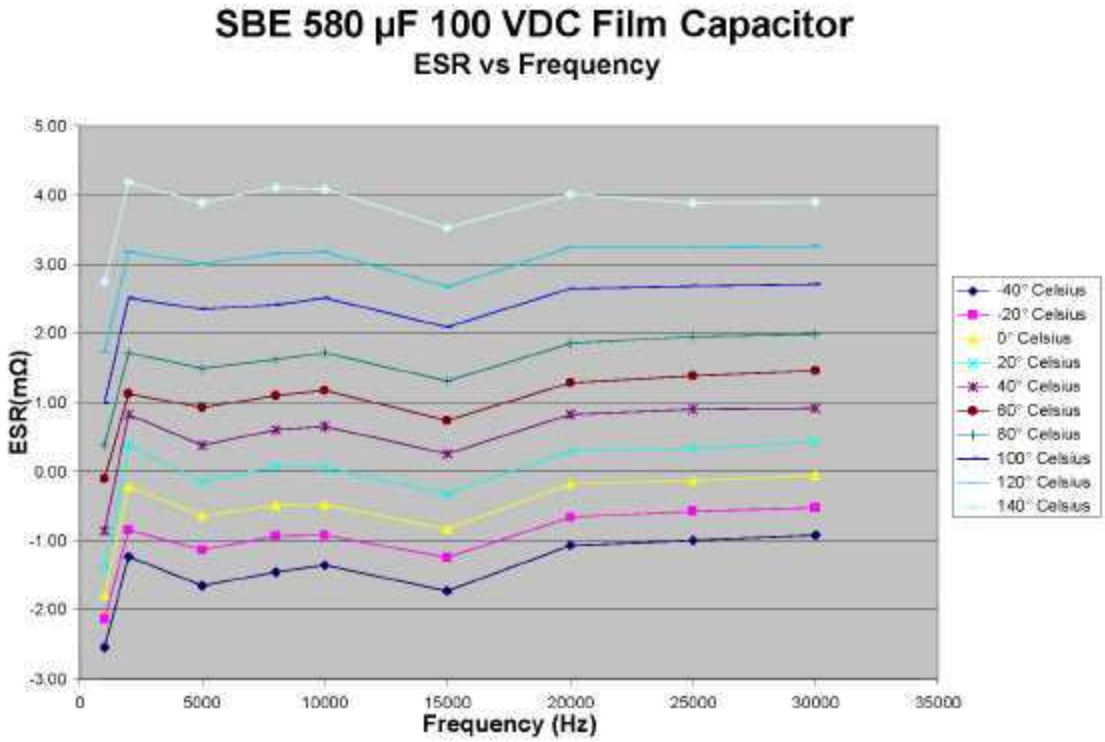


Fig. 2.14. SBE 580 µF film capacitor ESR frequency response.

An Agilent 4284 LCR meter was used to measure ESR, capacitance value, and DF for the static tests. The negative values shown here for ESR can be attributed to the LCR meter's method of measurement. An explanation from the manufacturer indicated that a capacitor with very low losses could fall in the + or – tolerance range and could display as negative. The geometry of the SBE film cap, as shown in Fig. 2.12, provides very little distance between the top and bottom; therefore, the ESR is very low at certain temperatures and frequencies.

At -40°C, the ESR increased 51% between 1–2 kHz. Between 2–30 kHz the ESR increased 25%. At 140°C, the ESR increased 52% from 1–2 kHz and decreased 6.7% from 2–30 kHz. Overall, the ESR response over frequency appears fairly flat if averaged over the entire range of frequencies tested.

Figure 2.15 plots the same ESR data versus temperature.

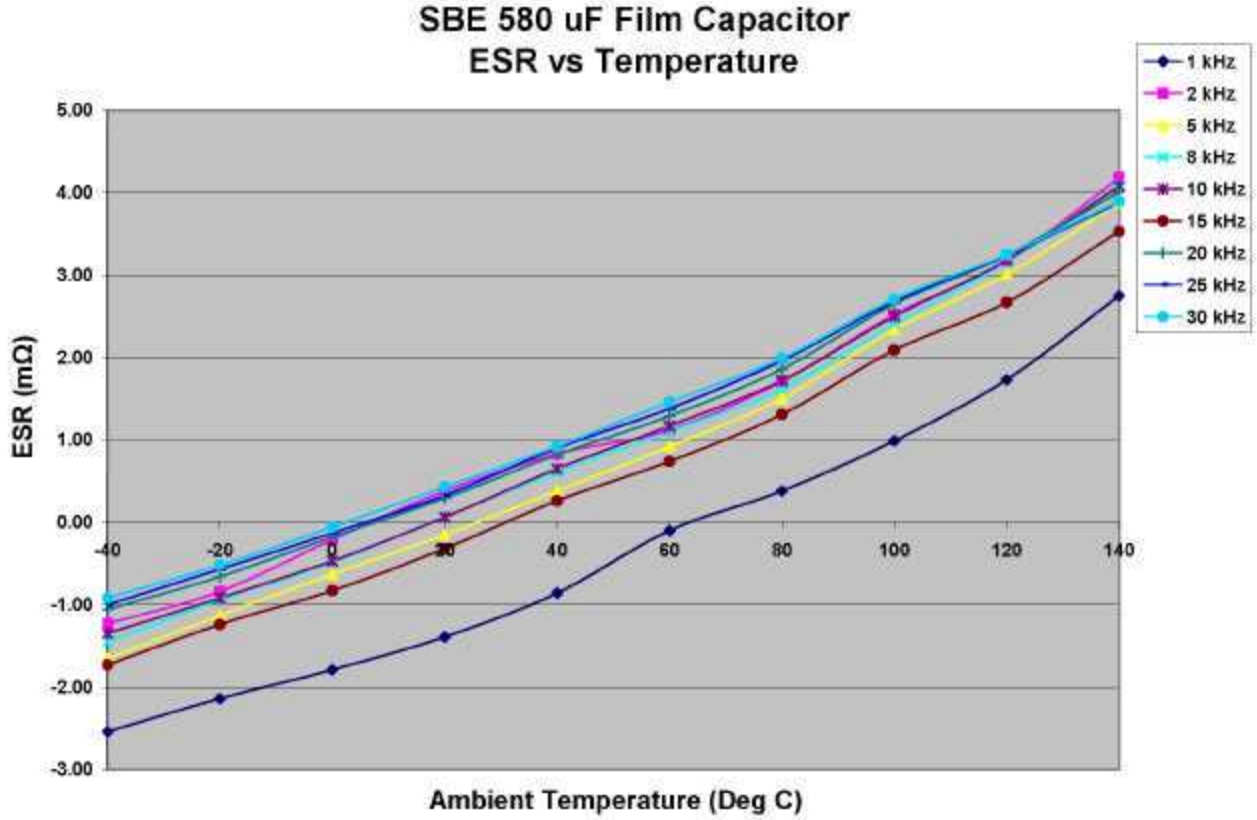


Fig. 2.15. SBE 580 µF film capacitor ESR temperature response.

From the data, a significant rise in ESR can be seen across the temperature range tested.

The ESR increased 5.29 mΩ at 1 kHz over the temperature range of -40–140°C. At 30 kHz, the ESR increased 4.82 mΩ over the temperature range of -40–140°C.

Figure 2.16 shows the capacitance response over the frequency range of 1–30 kHz at each temperature step.

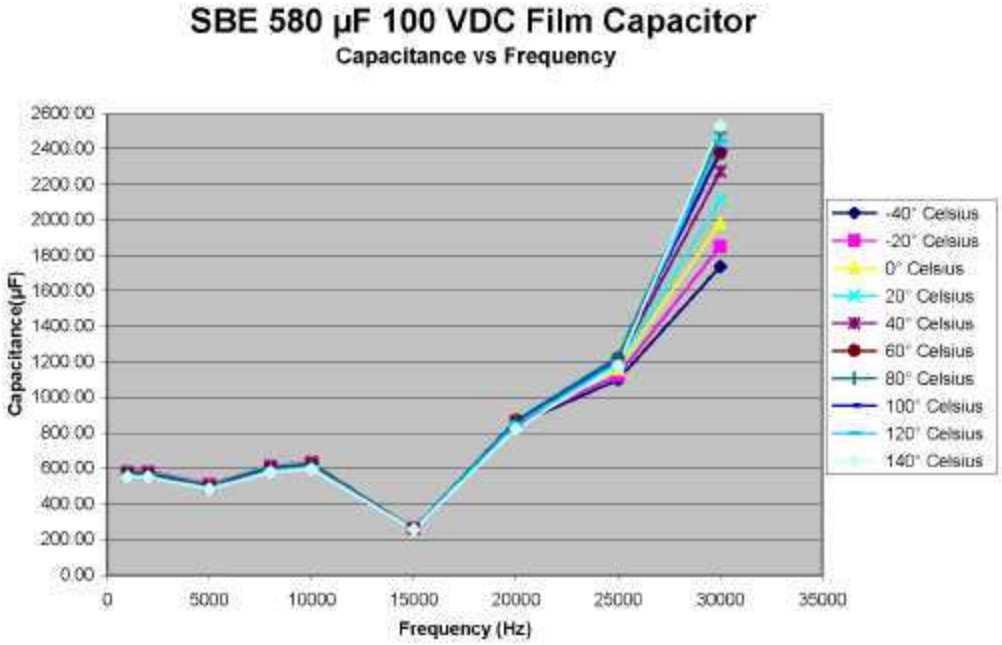


Fig. 2.16. SBE 580 µF film capacitor frequency response.

The rise in capacitance appears fairly significant at frequencies over 15 kHz. The capacitance decreased 55% from 1–15 kHz at -40°C, but increased 569% from 15–30 kHz at -40°C. The capacitance decreased 54% from 1–15 kHz at 140°C, but increased 892% from 15–30 kHz at 140°C.

Figure 2.17 graphs this data showing how the capacitance changes over temperature, while keeping the frequency constant.

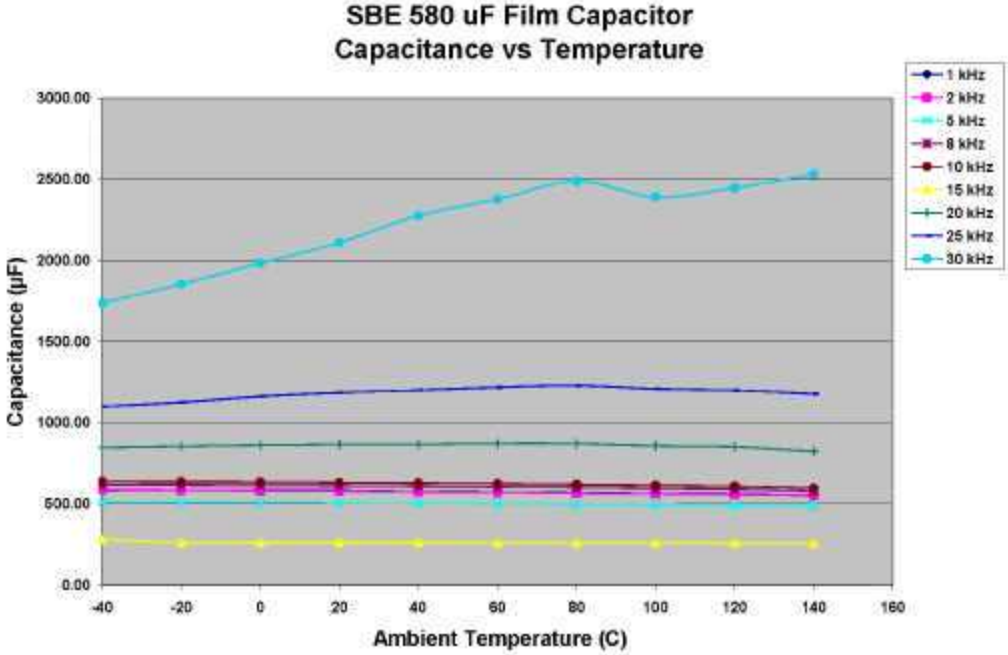


Fig. 2.17. SBE 580 µF film capacitor temperature response.

At 1 kHz, the capacitance changed from 584 µF to 552 µF, a decrease of 32 µF, over the temperature range of -40–140°C. At 30 kHz and -40°C, the capacitance value was 1739 µF. At 30 kHz and 140°C, the capacitance value had changed to 2531 µF, an increase of 792 µF over the temperature range of -40–140°C.

The capacitance value did not change in regard to temperature at or below 20 kHz. Above 20 kHz, the ambient temperature made a difference in the capacitance value. Lower temperatures produced less change in capacitance at higher frequency.

Figure 2.18 shows how the DF responded over the frequency range of 1–30 kHz at each temperature step between -40–140°C.

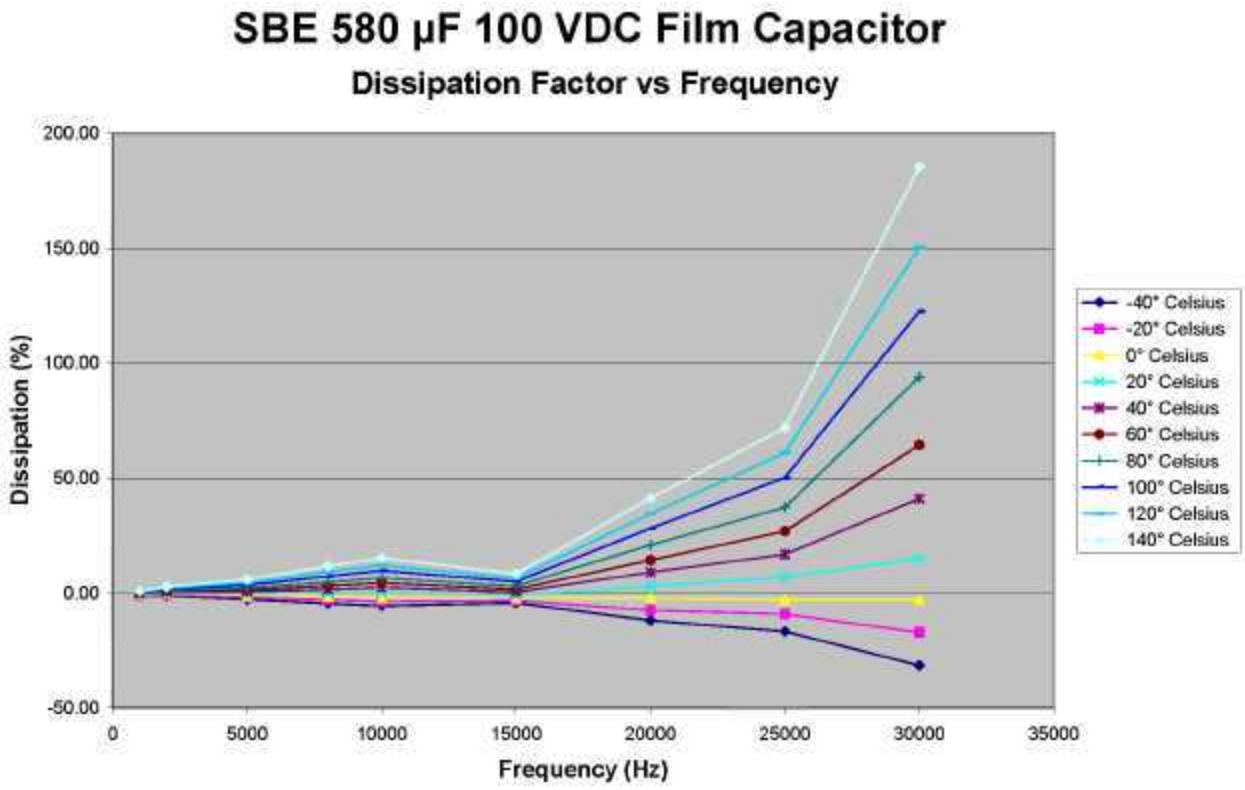


Fig. 2.18. SBE 580 µF capacitor DF frequency response.

These data indicates a negative DF at several temperatures, which is explained in the ESR data plot in Fig. 2.14. In discussions with the LCR manufacturer, if a capacitor has a very low loss, the ESR and DF could fall within the + and – tolerance range and be displayed as a negative number. The SBE film capacitor has a geometry that provides very low losses at certain temperatures and frequencies. Negative ESR and DF are not possible, so the absolute values of these data will be discussed relative to percent change in regard to temperature and frequency.

At -40°C, the DF decreased 367% from 1–15 kHz. From 15–30 kHz, the DF decreased 645%. At 140°C, the DF increased from .93–8.5 (810%) from 1–15 kHz. From 15–30 kHz, the DF increased from 8.5–185.5 (2082%) at 140°C.

Figure 2.19 graphs the DF over temperature from -40–40°C.

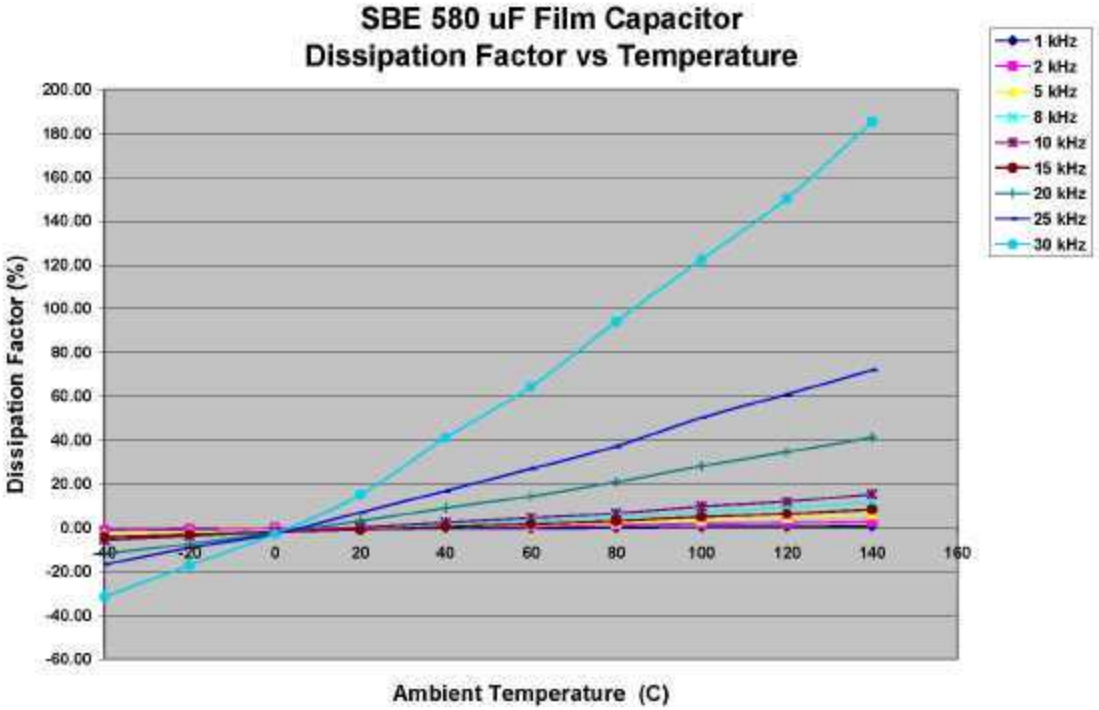


Fig. 2.19. SBE 580 µF film capacitor DF temperature response.

The DF for the SBE 580 µF film capacitor increased 1.84 units at 1 kHz over the temperature range of -40–140°C. The DF increased 216.79 units at 30 kHz over the same temperature range of -40–140°C.

The slope of the graph shows a considerable increase at the higher frequencies.

From these data it shows that higher temperatures at higher frequencies result in much higher DF. At temperatures below 20°C, the DF will decrease as the frequency increases. At temperatures of 20°C and higher, the DF will increase as frequency increases.

2.2.2 Dynamic SBE Tests

Ripple current tests were conducted on the SBE 580 µF 100 Vdc film capacitor at 20°C ambient. Figure 2.20 shows the test fixture and the thermocouples locations. Figure 2.21 shows the capacitor test fixture inside the environmental chamber.

Thermocouple number 2 is attached to the inside of the phenolic ring. Holes were drilled in three separate locations as recommended by SBE with depths half the thickness of the capacitor. Thermocouples 3, 4, and 5 are placed inside the holes at these locations. There is also a copper crush ring between the capacitor and each of the test fixture plates to ensure equal conduction between the plates and the capacitor to avoid hot spots.

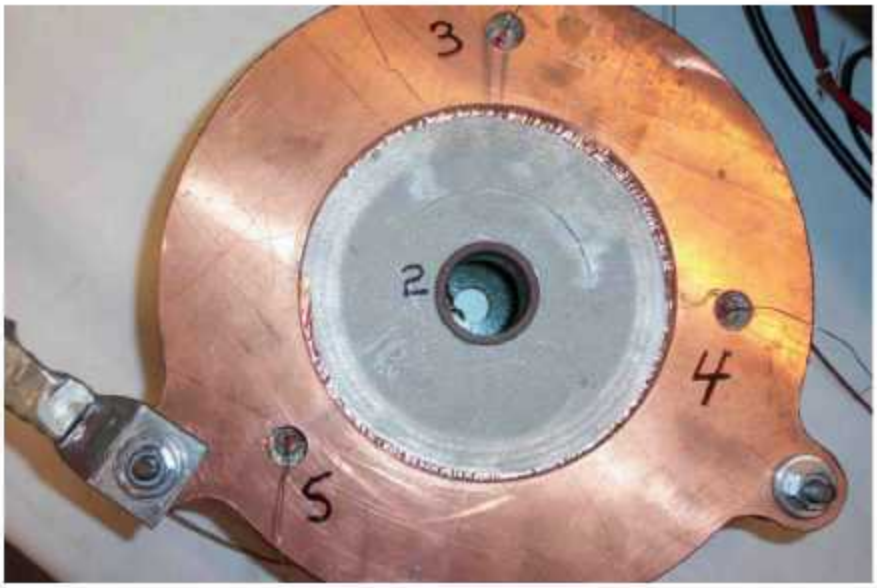


Fig. 2.20. SBE 580 µF capacitor thermocouple layout.

Fig. 2.21. SBE 580 µF film capacitor test fixture inside environmental chamber.

Figure 2.22 shows the ripple current versus temperature results for four different thermocouples at 20°C ambient temperature.

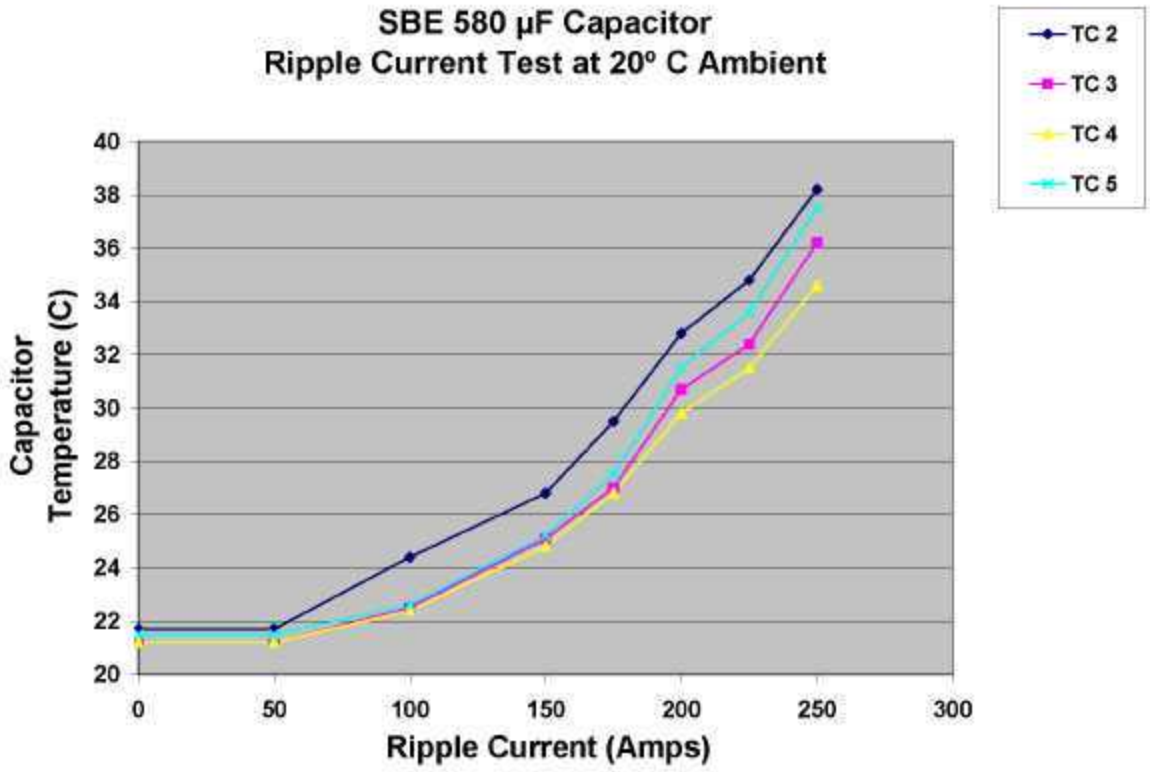


Fig. 2.22. SBE 580 µF film capacitor ripple current vs. temperature.

The ripple current tests were done at 4 kHz with a maximum current of 250 A. Thermocouple number 2 increased 76% with a maximum temperature of 38.2°C at 250 A. The average increase of thermocouples 3, 4, and 5 was 69% with an average maximum temperature of 36.1°C at 250 A.

3. INFINEON TRENCH 150°C JUNCTION TEMPERATURE IGBT TESTS

Task: Test the performance of the Infineon FS30R06W1E3 trench technology IGBTs across a wide temperature range (25–200°C).

3.1. EXPERIMENTAL SETUP

Figure 3.1 Shows details of an Infineon IGBT pack FS30R06W1E3 layout.

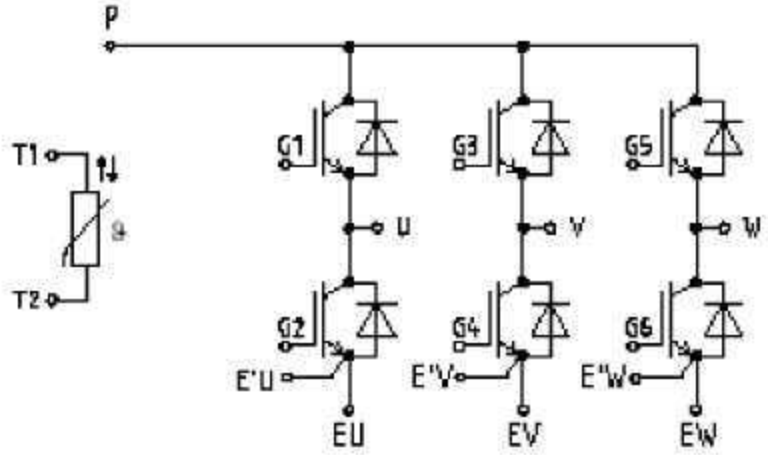


Fig. 3.1. Layout of the Infineon IGBT module.

Figure 3.2 shows the test schematic. Only one leg of the IGBT module was utilized for the test. The other two legs were left 'floating.' A 300V, 200A dc power supply was used for Vdc. The power supply was connected across the P and EU terminals, shown in Fig. 3.1. The load was connected across the first IGBT between the P and U terminals. The load was comprised of 28mH's (4mH × 7) of inductance rated for 40A and 300W of variable resistors.

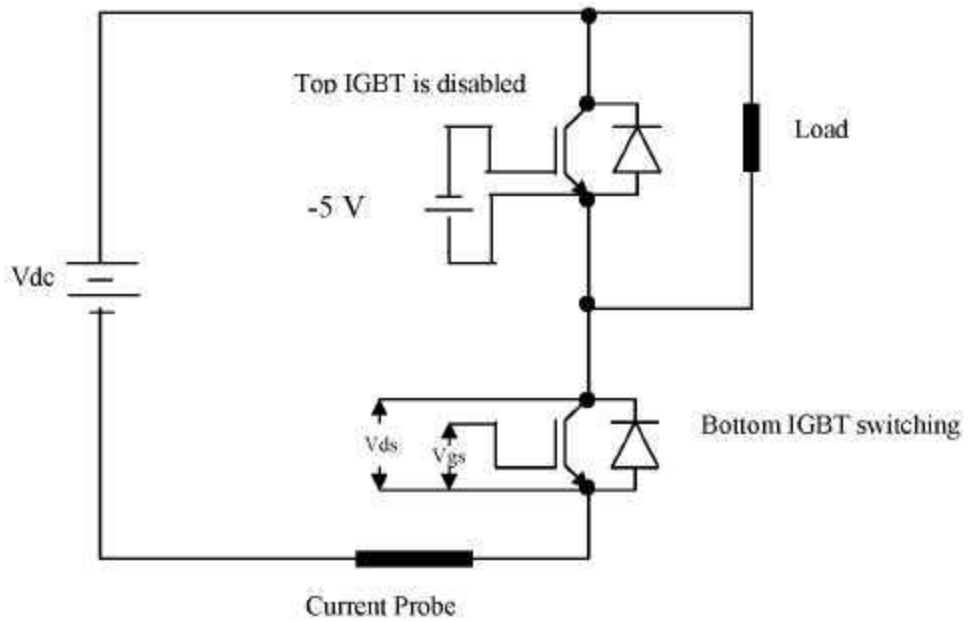


Fig. 3.2. Schematic of the circuit.

The upper IGBT was turned OFF by supplying -5V between the gate and the source (i.e. between the G1 and U terminals) referencing Fig. 3.1. A Fuji EXB840 chip was used as the gate driver. The lower IGBT was hard switched, no snubber was utilized. An Agilent 33250A waveform generator was used to generate the 5 kHz switching frequency with a duty cycle of 20%. The voltage was measured across the drain and the source (between the U terminal and E'U terminals of Fig 3.1) of the lower IGBT. A Tektronix TCP404XL current probe was used along with a TCPA400 current amplifier to measure the lower IGBT source current. A Tektronix TDS 5104B oscilloscope was used to monitor and record the various current and voltage waveforms. The setup is shown in Fig. 3.3(a).

As shown in Fig. 3.3(b), a Fisher Scientific Isotemp hot plate was used to vary the junction temperature of the IGBT. The IGBT module was mounted on a copper plate, which was glued to the hot plate using thermal grease. The temperature of the hot plate was measured and fed back using a thermocouple to control the desired temperature.

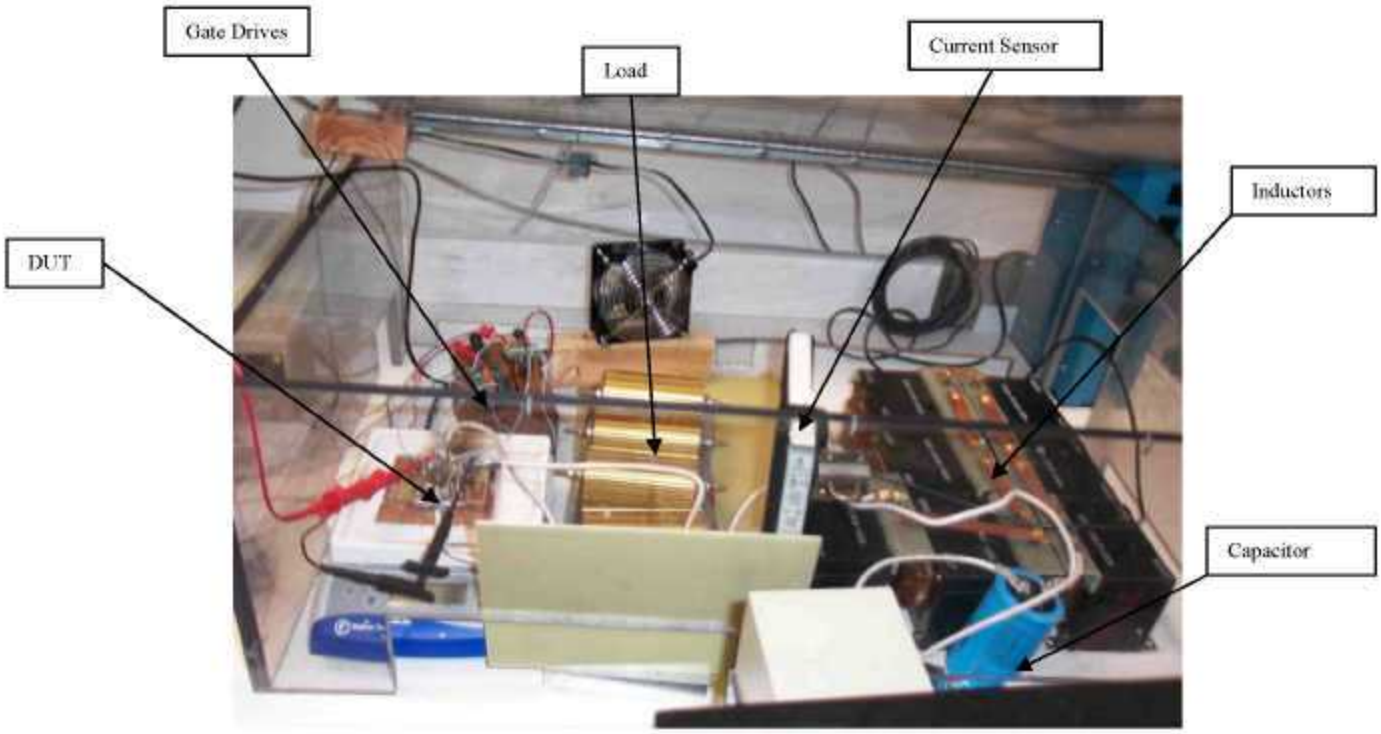
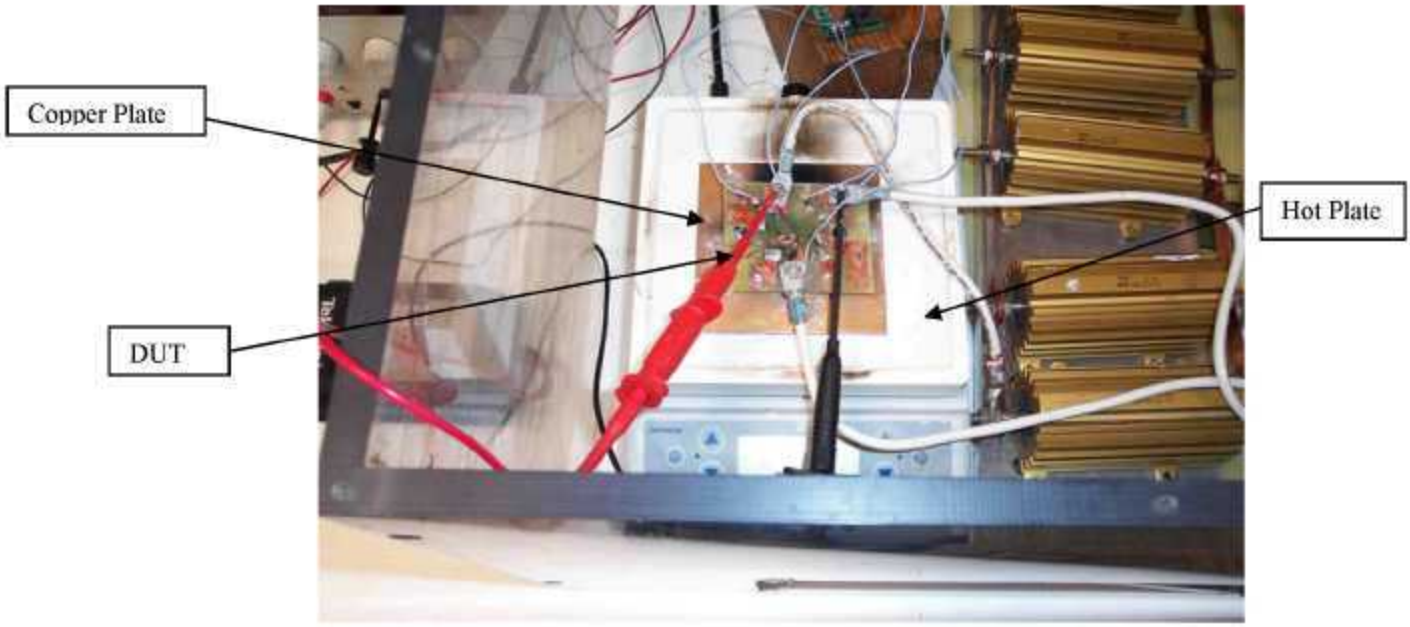


Fig. 3.3(a). Test setup.



(b)

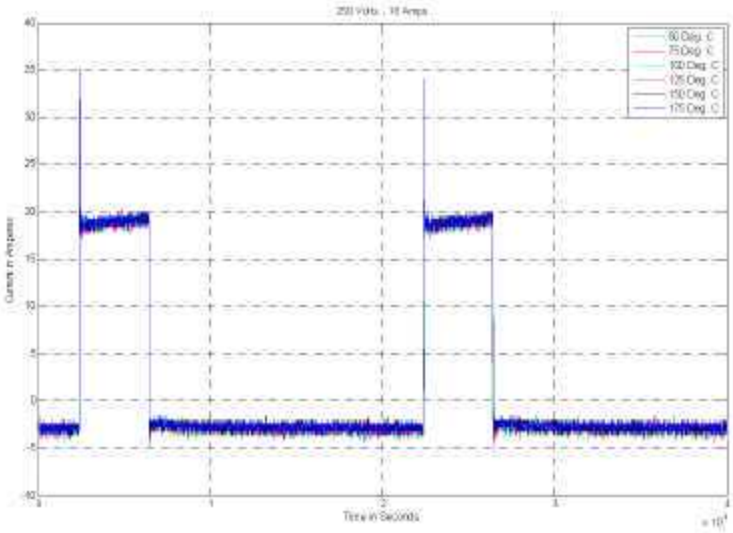
Fig. 3.3(b). Test setup (closer view).

3.2 TEST PROCEDURE

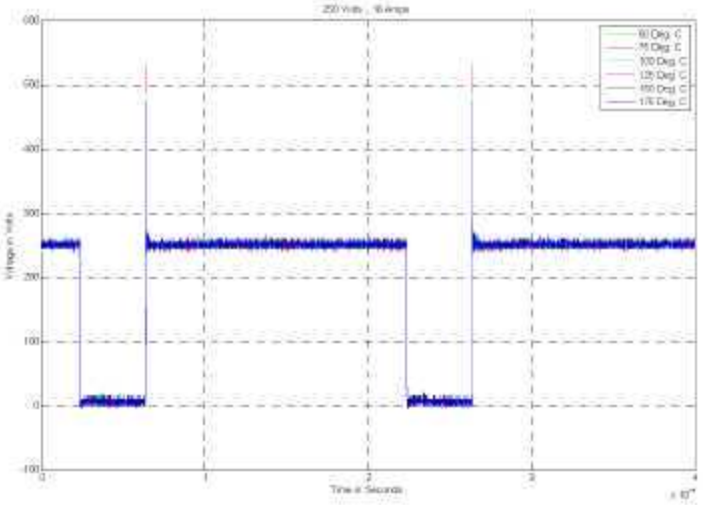
- Connect the desired value of resistance (10Ω, 5Ω, 3.33Ω, 2.5Ω, 2.20Ω, and/or 1.8Ω) by connecting 20Ω, 300 W resistances in parallel.
- Slowly increase Vdc to 250V.
- Record the current and voltage waveform at different temperatures in steps of 25– 200°C.
- Increase the current in steps of 5; from 5A 10A, 15A, 20A, 25A to 30 A to supply continuous dc current.

3.3 RESULTS

Some of the graphs obtained from the data recorded are shown in Figs. 3.4–3.6.

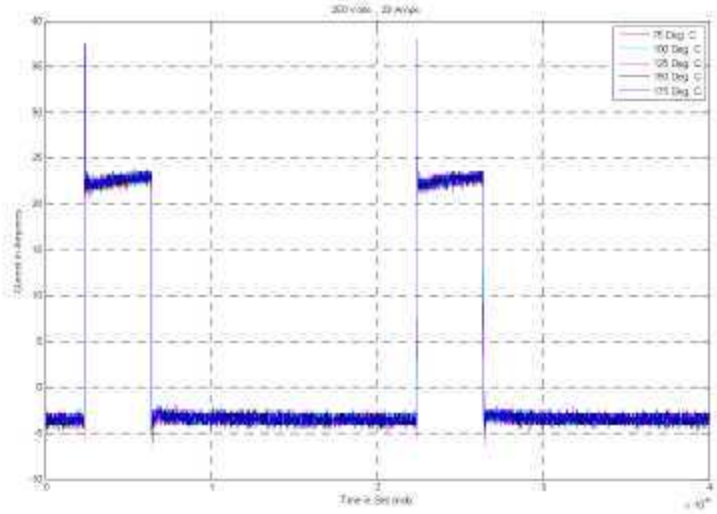


(a)

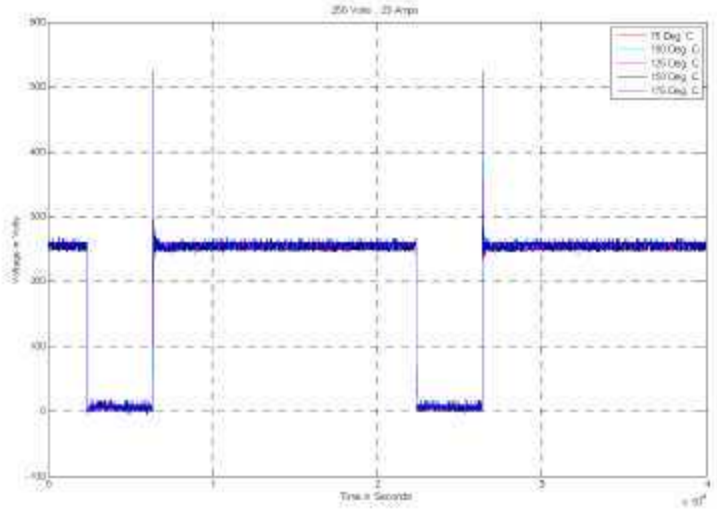


(b)

Fig. 3.4. (a) Current for 250V, 16A operation; and (b) Voltage for 250V, 16A operation.

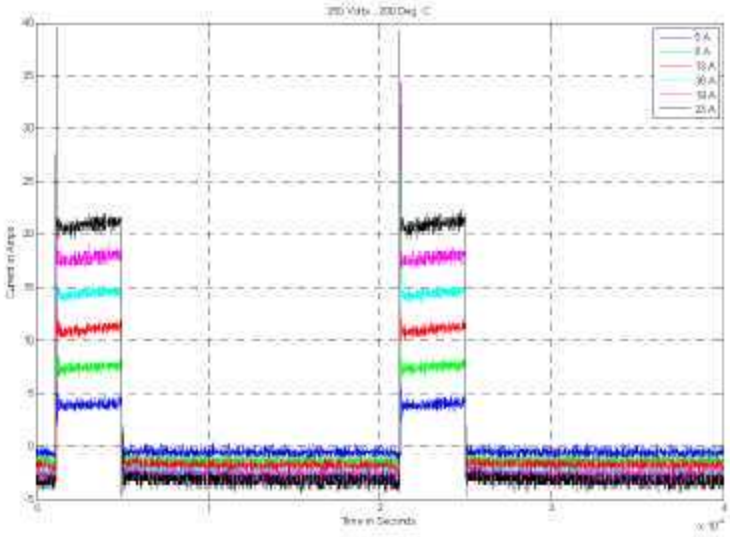


(a)

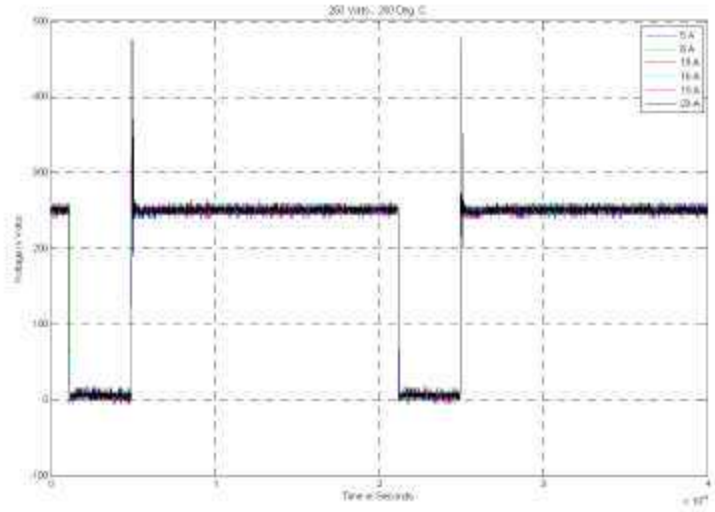


(b)

Fig. 3.5. (a) Current for 250V, 23A operation; and (b) Voltage for 250V, 16A operation.



(a)



(b)

Fig. 3.6. (a) Current for 250V, 200°C case temperature operation; and (b) Voltage for 250V, 200°C case temperature operation.

It should be noted that the devices were operated without any snubbers in the circuit. The voltage spikes seen in the waveforms are due to the hard switching of the devices without any snubbers. The IGBT failed while operating at 250V and 16A with a case temperature of 200°C after approximately 10 minutes, as shown in Fig. 3.7. Similar steps were carried out on different legs of the module to confirm the failure. A second IGBT failed at 250 V, 23 A while operating with a case temperature of 200°C.

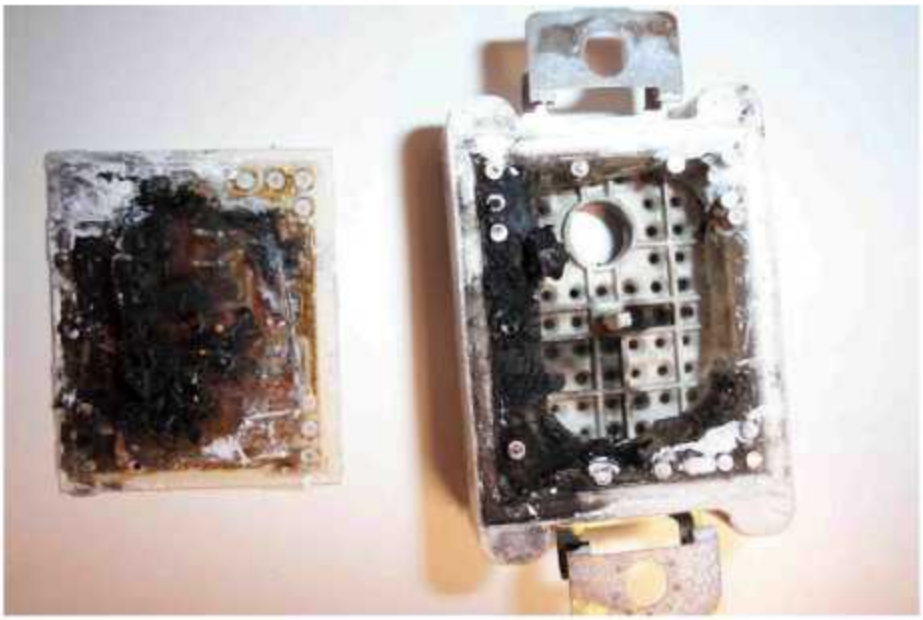


Fig. 3.7. Device failure at 250V, 16A, 200°C case temperature.

3.4 CONTINUOUS DC CURRENT TEST

In this test, (10) 20Ω, 300W resistors were connected in parallel to obtain a total of 1.8 Ω resistance. Voltage was increased in order to obtain current steps of 5, 10, 15 20, 25, and 30 A. Tests were carried out at 50, 100, 150, 175, and 200°C case temperatures. One device failed at 30A while operating at 200°C case temperature after approximately 5 minutes. Similar tests were carried out on a different IGBT leg to confirm the failure point. This leg also failed at 30A, with a case temperature of 200°C.

3.5 CONCLUSION

The devices performed without failures up to 175°C junction temperature under different load conditions. The test devices were switched at 5kHz, 20% duty cycle, 250V, and 23A (38 A peak transients) without any problems (refer to Fig. 3.5). The devices were operational with different load conditions for at least 15 minutes at each data point. After increasing the case temperature to 200°C, one device failed after 10 minutes of operation with 16A of load current (refer Fig. 3.7). A second test device failed at 23A load current while operating at a case temperature of 200°C.

The devices were subjected to continuous dc current tests to study the performance of the devices close to the rated current. The devices operated without failures at the rated current of 30A and 175°C case temperature. These test conditions were maintained for 15 minutes of operation. However, when the case temperature was raised to 200°C the device operated satisfactorily at 25A and then failed at 30A of load current. The tests were repeated to confirm the failure point and the second device failed again at 30A load current.

It can be concluded that the device is capable of operating at 175°C without derating of the continuous current rating. However, at operation with a case temperature of 200°C the devices failed during both switching tests and dc tests below the rated current.

4.0 OPAL-RT TEST SETUP

The control system necessary for module level testing consists of two computers connected by an ethernet cable. One is a Windows based system (Command Station) and is the control computer that the user interfaces with. The other (Target Node) is QNX OS supplied with Opal, which is a real-time operating system (RTOS) dedicated computer with I/O cards that actually performs the control. This Target Node computer contains all the digital and analog I/O hardware to the DUT.

The Opal-RT system consists of a suite of programs that interface and build upon one another. Therefore all programs (with their respective licenses) need to be on the Command Station computer for development efforts. For execution only, just RT-LAB needs to be on the Command Station. The control code is entered in MATLAB/Simulink and the resultant compiled code is processed by RT-LAB to be loaded on the Target Node(s). In systems with more than one Target Node, the executable code needs to be split up among the various Target Nodes by the user. However, in the ORNL configuration only one Target Node is utilized so all executable code is loaded on the same Target.

4.1 DEVELOPMENT PROCESS

Users who wish to develop or alter code need to be familiar with MATLAB/Simulink in order to develop or change the control code. MATLAB is a technical computing software package that integrates programming, calculation, and visualization. Simulink is a software package that enables modeling, simulation, and analysis of dynamic systems. The models are described graphically following a precise format based on a library of blocks. RT-LAB uses Simulink to define models that will be executed by the real-time multiprocessing system and defines its own simulation parameters through Simulink.

Full development of a new model or even the modification of a current model requires good working knowledge of the entire suite of Opal-RT and Matlab. The operation of the RT-LAB for controlling power electronics assumes the system has been fully implemented both in hardware and software and only the operation of the control for running tests is described here.

In addition to knowledge about Matlab/Simulink, the user should consult the Opal-RT manual for specific requirements of RT-LAB such as subsystem requirement of master, slave, and console. To edit an existing controller model, follow steps 1 and 2 in the test procedure below. Then click "Edit" to load Matlab/Simulink and wait about one minute for the model to be opened. Make any necessary changes. After the file is saved, click "Compile" to compile the convert the real-time model and be on alert for any compilation warnings or errors. Follow steps 3–5 below to load and execute the controller program.

4.2 TEST PROCEDURE

In the following test procedures, bold indicates control buttons on Main Control Panel:

1. Call RT-Lab Main Control panel up with icon in far right Window's task bar.
2. **Open** module to load on Target in C:\TAB\Simulink\(prog dir)*.mdl.
3. **Load**. Insure message panel has no errors. If so fix.
4. Turn on Inverter with manual switch or 15V power supply. This needs to be done before turning on the controller.
5. **Execute** code on Target. It will take two-three seconds for response.
6. To change **Parameters**:
   a. Revolutions per minute (**rpm**) is target speed in rpm.

b. **rpmrate** is acceleration in radians/sec to get to rpm. For deceleration, unit will just coast to target rpm.

7. Shutdown Inverter enable first before reset of control program via manual switch or 15V power supply.
8. Reset only after motor under test coasts to zero.
9. To restart go to step 3 above.

Notes:
Be sure to turn on inverter enable before executing Target control code and turn it off before Reset of control program.

CPU fan on Target node has a tendency to fail causing Target computer to quit in middle of testing. Insure backup to CPU cooling.

4.3 CALIBRATION OF EQUIPMENT

It was necessary to perform calibration of laboratory equipment in order to accurately test components and potential high temperature power electronic modules. During the year various pieces of equipment were sent for calibration to support ORNL's extensive test efforts, as well as high temperature component benchmarking.

Table 4.1 lists the complete equipment list that was calibrated to support ORNL high temperature test efforts in FY07.

Table 4.1. Equipment list that was calibrated to support ORNL high temperature test efforts in FY07

DESCRIPTION	SERIAL NUMBER
Yokogawa 2531 series power meter with harmonics measurement, model#2531-30-C2-3-D/HRM	24AW2056
Yokogawa PZ4000 power meter actual model# 253710-D/B5/C7/M3	27CC16078M
Agilent 3458A high accuracy Digital Voltmeter	US28031302
Agilent 35670A Dynamic Signal Analyzer options 1C21D01D11D21D31D4AY6	MY42506754
Tektronix TDS5104B 4 channel Digital Phosphor oscilloscope	B010713
Tektronix TDS5104B 4 channel Digital Phosphor oscilloscope	B021145
Yokogawa DL7480 8 channel analog 16 ch. Digital oscilloscope acutal model# 701480-D-J2/B5/E4/N4/C7/C10/G2/P4	27D232620B
Yokogawa DL7480 8 channel analog 16 ch. Digital oscilloscope acutal model# 701480-D-J2/B5/E4/N4/C7/C10/G2/P4	12C813404 H
F.W. Bell/Sypris model 7010 Gauss/Teslameter - .05% accuracy	335020
F.W. Bell/Sypris T-71-116 transverse probe	03A0102
F.W. Bell/Sypris STM71-0204-15-T transverse probe	460011
FWBell/Sypris VT-500 reference magnet 500 gauss-transverse	329445
FWBell/Sypris VT-10K reference magnet 10K gauss-transverse	329447
FWBell/Sypris VA-2K reference magnet 2Kgauss-axial	329448
Yokogawa DL750 scope/recorder model# 701210-D-J2/HE/M3/C8/C10/G2/G3	27D510633D
Yokogawa 701251 - 16 bit 1MS/Sec. isolation module for DL750	27D405647D
Yokogawa 701251 - 16 bit 1MS/Sec. isolation module for DL750	27D405657D
Yokogawa 701271 dual strain gauge module for DL750	27D520396E
Yokogawa 701271 dual strain gauge module for DL750	27D520395E
Yokogawa 701260 module-16bit 100KSa/Sec. isolated	27D231318
Yokogawa 701260 module-16bit 100KSa/Sec. isolated	27D341527
Yokogawa 701260 module-16bit 100KSa/Sec. isolated	27D341526
Yokogawa 701250 module- 12 bit isolation, 10 Msa/Sec.	27D422251
Yokogawa 701250 module - 12 bit isolation, 10 Msa/Sec.	27D341344
Yokogawa 701250 module - 12 bit isolation, 10 Msa/Sec.	27D341345
Yokogawa 701265 module	27D222124B
Yokogawa 701265 module	27D222125B
Yokogawa 701265 module	27D222130B
Yokogawa 701265 module	27D222131B

5. SiC DEVICE TESTING

A portion of the funding provided for this effort was allocated to support wide-bandgap (WBG) device characterizations. The complete report on this effort is documented in the ORNL annual report in the "Wide-Bandgap Materials" section. It is included in Appendix A.

6. RELIABILITY OF POWER ELECTRONICS PACKAGING TECHNIQUES

As part of this effort a subcontract with Pat McCluskey of Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland was initiated to investigate power module packaging reliability issues with operation at high temperatures. The entirety of the report is attached in Appendix B.

7. CONCLUSIONS

As a result of funding remaining from an effort by Semikron on the development of a high temperature inverter designed to operate with 105°C coolant, several tasks were performed by ORNL to examine the viability of high temperature components for use in such a module. Findings from Semikron during their work revealed that one of the main challenges of this work was obtaining capacitors with sufficient capabilities at the elevated temperatures. As a result of this several capacitor technologies were examined and tested for possible use in high temperature power electronics. SiC components and new high temperature silicon (Si) IGBTs were also evaluated to assess their reliability and characteristics at elevated temperatures and under fault conditions.

In order to perform accurate performance evaluations of components and modules calibrations of select laboratory equipment and software modifications to the existing test beds in the Power Electronics and Electric Machinery Research Center (PEEMRC) laboratory were made.

Finally, a detailed study on existing power module packaging techniques was performed to identify limitations on current methods and provide insight into their use in high temperature applications for future advanced vehicles.

APPENDIX A: WIDE-BANDGAP MATERIALS

A.1. TASKS

- Assess the impact of replacing Si power devices in transportation applications with devices based on WBG semiconductors, especially SiC.
- To study the impact of SiC devices on PHEVs.
- To study the possibility of using a thermal boundary in SiC intelligent power modules (IPMs) where Si gate drivers can be used.
- To study the fault current limiting capability of SiC devices for safety and protection.

A.2 APPROACH

- Develop models of WBG semiconductor devices, junction field-effect transistors (JFETs), and metal oxide semiconductor field-effect transistors (MOSFETs).
- Integrate Si-based and SiC-based inverter loss models into a drive train using PSAT software to compare the impact of replacing Si devices with SiC devices.
- Develop a hybrid device package and simulate the model to study the feasibility of using a thermal boundary in SiC-based IPMs.
- Develop circuits to study the fault current limiting capability of SiC devices.

A.3 MAJOR ACCOMPLISHMENTS

- Acquired several SiC Schottky diodes, JFETs, and SiC MOSFETs.
- Tested, characterized, and modeled SiC Schottky diodes, JFETs, and MOSFETs.
- Developed and modeled a hybrid device package.
- An inverter loss model was successfully integrated into the drive train model in PSAT.

A.3.1 Technical Discussion

A.3.1.1 Device testing

Several new WBG devices were acquired this year and these devices were tested, characterized, and modeled. The devices included SiC JFETs, SiC MOSFETs, and SiC Schottky diodes. All the devices obtained were experimental samples. A high temperature Si IGBT was also tested this year to verify the claims of high temperature. Tables A.1 and A.2 below show results of some of the WBG devices tested from 2004–2007.

Table A.1. Power diodes

Device Type	Ratings	On-Resistance (Ω)	Forward Voltage Drop (Volts)	Manufacturer	Year Tested
SiC Schottky Diode	1200 V, 7.5 A	0.15 Ω at -50°C to 0.32 Ω at 175°C	1.42 V at -50°C to 1.21 V at 175°C	Vendor A	2004
SiC Schottky Diode	300 V, 10 A	0.15 Ω at -50°C to 0.16 Ω at 175°C	1.11 V at -50°C to 0.83 V at 175°C	Vendor B	2004
SiC Schottky Diode	600 V, 4 A	0.19 Ω at -50°C to 0.39 Ω at 175°C	1.09 V at -50°C to 0.87 V at 175°C	Vendor C	2004
SiC Schottky Diode	600 V, 10 A	0.14 Ω at -50°C to 0.25 Ω at 175°C	1.09 V at -50°C to 0.82 V at 175°C	Vendor C	2004
SiC Schottky Diode	600 V, 75 A	0.01 Ω at -50°C to 0.03 Ω at 175°C	0.91 V at -50°C to 0.61 V at 175°C	Vendor C	2005
GaN Schottky Diode	600 V, 4 A	0.23 Ω at 25°C to 0.47 Ω at 175°C	0.83 V at 25°C to 0.67 V at 175°C	Vendor D	2006
SiC Schottky Diode	600 V, 6 A	0.138 Ω at 50°C to 0.359 Ω at 300°C	0.745 V at 50°C to 0.365 V at 300°C	Vendor E	2007

Table A.2. Power switches

Device Type	Ratings	On-Resistance (Ω)	Voltage Drop at Rated Current @ Room Temperature (Volts)	Manufacturer	Year Tested
SiC JFET	1200 V, 2 A	0.36 Ω at -50°C to 1.4 Ω at 175°C	1.3 V @ Vgs = 0 V	Vendor F	2004
SiC JFET	1200 V, 10 A	0.25 Ω at -50°C to 0.58 Ω at 175°C	2.71 V @ Vgs = 0 V	Vendor F	2006
SiC JFET	1200 V, 15 A	0.15 Ω at -50°C to 2.2 Ω at 175°C	3.2 V @ V_{gs} = 3 V	Vendor A	2006
SiC JFET	600 V, 5 A	0.26 Ω at -50°C to 1.87 Ω at 175°C	2.25 V @ V_{gs} = 3 V	Vendor G	2006
SiC MOSFET	1200 V, 5 A	(0.48 Ω at -50°C to 0.23 Ω at 50°C) (0.24 Ω at 75°C to 0.29 Ω at 175°C)	1.5 V@ V_{gs}= 20 V	Vendor C	2005
SiC MOSFET	800 V, 10 A	0.25 Ω at 25°C to 0.09 Ω at 150°C	1.8 V@ V_{gs}= 15 V	Vendor C	2007
SiC JFET	600 V, 2 A	0.25 Ω at 25°C to 1.07 Ω at 200°C	1.3 V@ V_{gs}= 0 V	Vendor G	2007

A.3.1.1.1 *SiC Schottky diode*

Static Characteristics

A 600V/ 6 A SiC Schottky diode packaged in a high temperature package was obtained from Sienna Technologies. The main objective was to determine the performance of the diode at higher temperatures which would not be possible with a standard package. I-V characteristics of the diode were obtained at different temperatures in the 50–300°C temperature range (Fig. A.1). Figure A.2 shows the reverse characteristics of the diode over a wide temperature range. The blocking voltage decreases with increasing temperature. The leakage current increases with increasing temperature (Fig. A.3).

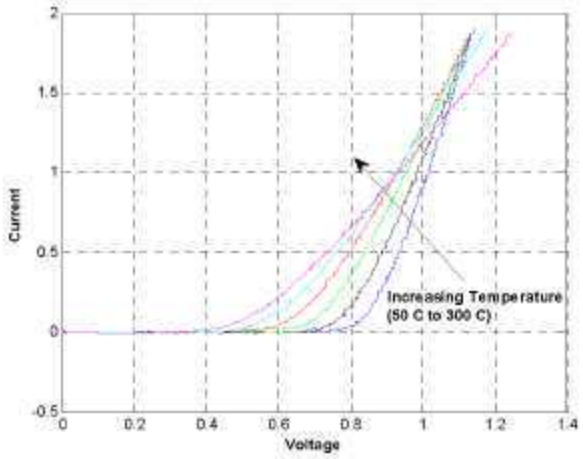


Fig. A.1. Forward characteristics.

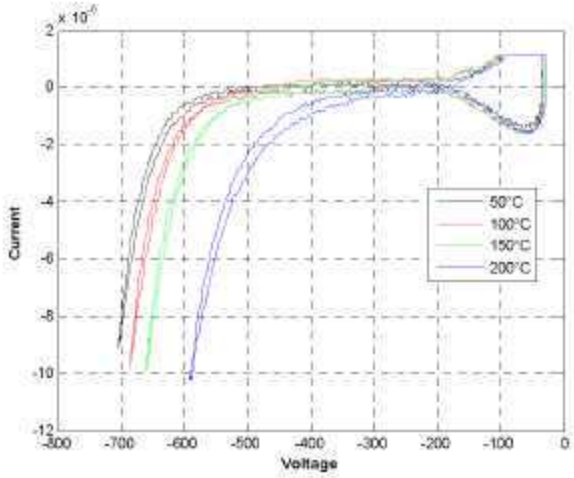


Fig. A.2. Reverse characteristics.

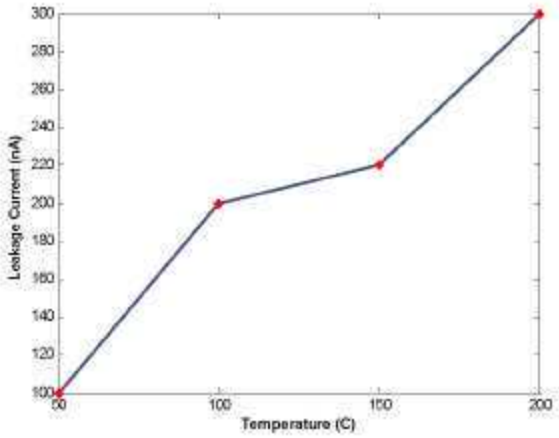


Fig. A.3. Leakage current of a SiC Schottky diode at different temperatures at 600 V.

Dynamic Characteristics

The SiC Schottky diode was also tested in a chopper circuit, shown in Fig. A.4, to observe its dynamic characteristics. The IGBT was switched at 1 kHz with a duty cycle of 50% and an R-L load. The reverse recovery tests were performed at different voltages and currents.

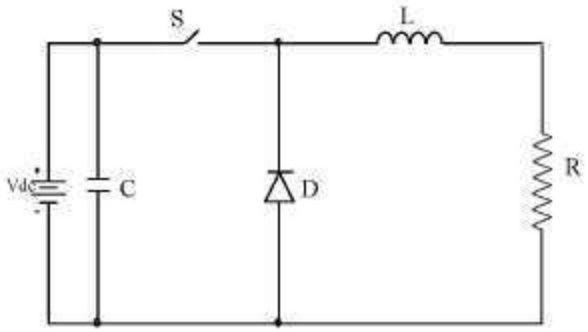


Fig. A.4. Reverse recovery test circuit.

The reverse recovery current waveforms obtained at different temperatures are shown in Fig. A.5. As seen in this figure, the reverse recovery current does not change much with temperature. Note that theoretically, Schottky diodes do not display reverse recovery phenomenon because they are majority carrier devices and do not have stored charge. The switching losses obtained at different temperatures are shown in Fig. A.6.

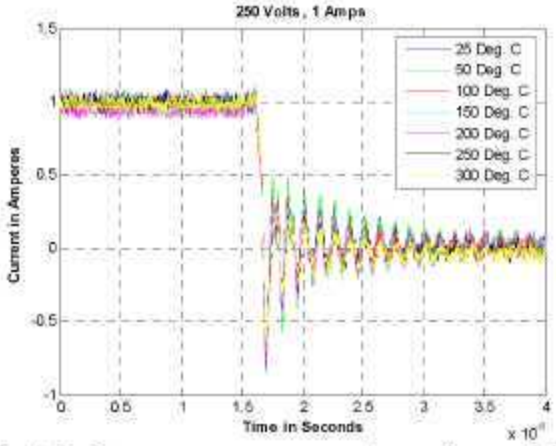


Fig. A.5. Reverse recovery current waveforms of the SiC Schottky diode at different temperatures.

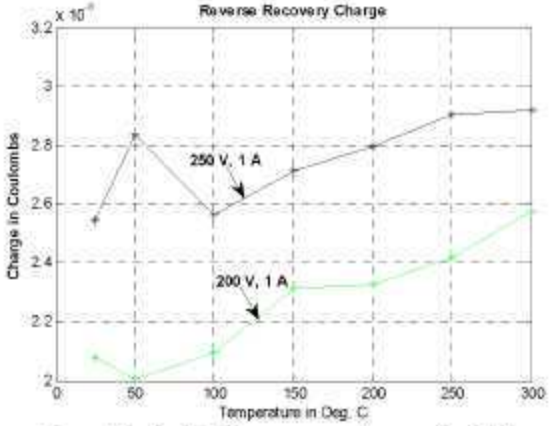


Fig. A.6. Switching energy losses of a SiC diode at different temperatures.

A.3.1.1.2 *SiC MOSFET*

The static characteristics of a (800 V, 10 A) SiC MOSFET for different operating temperatures are shown in Fig. A.7. This experimental device has a negative temperature coefficient unlike the earlier experimental samples which had both positive and negative temperature coefficients [A.1]. The on-resistance of the device decreases from 0.25 Ω at 25°C to 0.09 Ω at 150°C as shown in Fig. A.8. The transfer characteristics of the MOSFET, obtained for different temperatures, are shown in Fig. A.9.

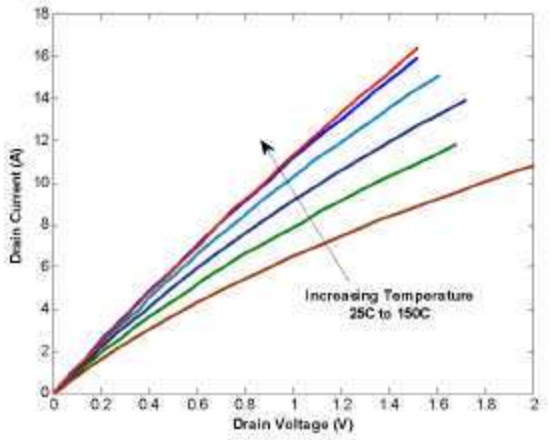


Fig. A.7. I-V curves of SiC MOSFET.

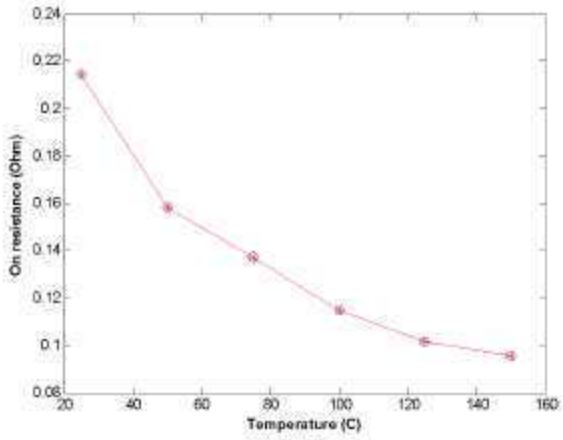


Fig. A.8. On-resistance of SiC MOSFET.

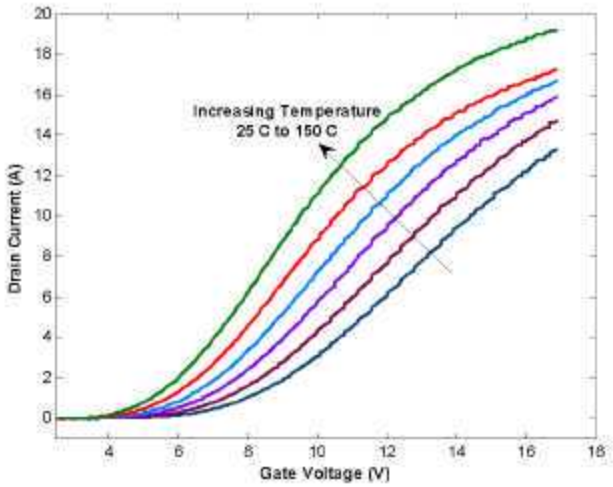


Fig. A.9. Transfer characteristics of SiC MOSFET.

Dynamic Characteristics

The SiC MOSFET was also tested in a chopper circuit with double pulse switching to observe its dynamic characteristics. The double pulse circuit enables the use of an inductive load instead of the combined resistive and inductive load. The current through the inductor builds up during the first pulse and peak forward current is adjusted by changing the width of the first pulse. The switch is turned-off and turned-on for short periods after the first pulse. The turn-on and turn-off energy losses can be obtained during the short pulse intervals.

The turn-on and turn-off switching energy losses of the MOSFET are shown in Fig. A.10. The turn-off losses do not change much with temperature but the turn-on losses decrease with increasing temperature.

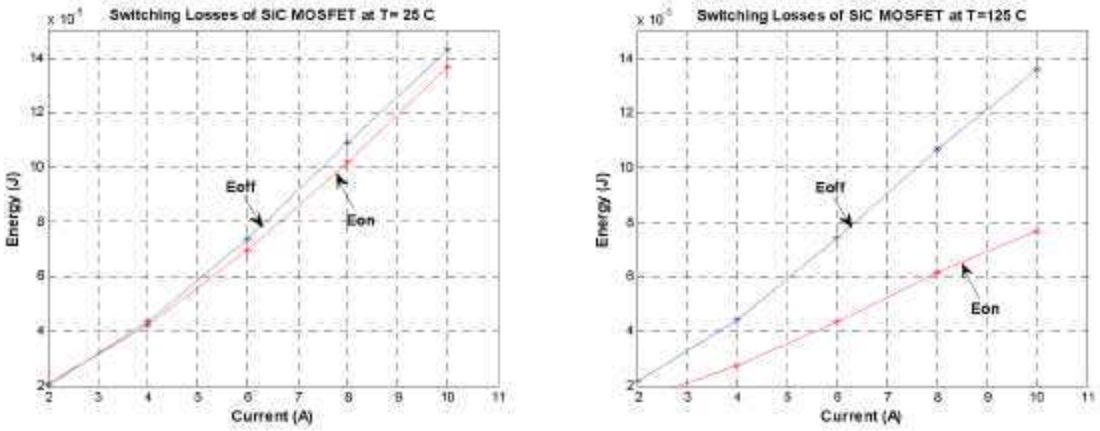


Fig. A.10. Switching energy losses of SiC MOSFET for different currents and temperatures.

A.3.1.1.3 *SiC JFET*

Static Characteristics

Static characteristics of a (600 V, 5 A) SiC JFET are shown in Fig. A.11 for different operating temperatures. SiC JFETs have a positive temperature coefficient which means that like SiC Schottky diodes, their conduction losses will be higher at higher temperatures. However, a positive temperature coefficient makes it easier to parallel these devices and reduce the overall on-resistance. The on-resistance of the JFET increases from 0.25 Ω at 25°C to 1.07 Ω at 200°C as shown in Fig. A.12.

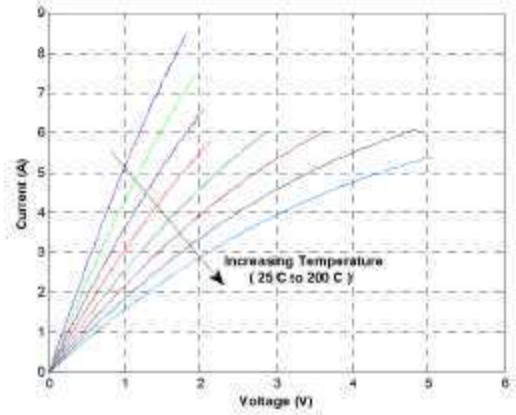


Fig. A.11. I-V curves of a SiC JFET.

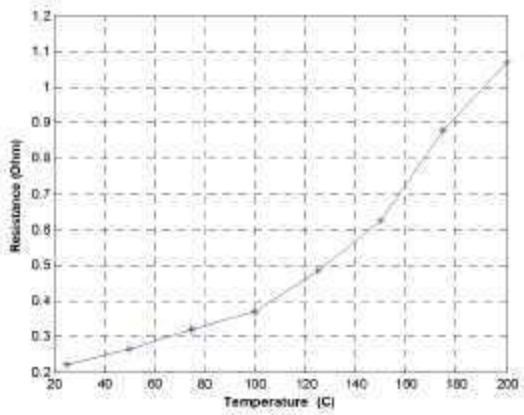


Fig. A.12. On-resistance of a SiC JFET.

A.3.1.1.4 *High temperature Si IGBT*

A high temperature Si IGBT module (FS30R06W1E3) was obtained from Infineon. These new Infineon trench technology based IGBTs are designed for operation at 175°C junction temperature. The objective of testing this device is to evaluate the performance of the IGBT over a wide temperature range (25–200°C). The static characteristics of the IGBT at different temperatures are shown in Fig. A.13. The IGBT has a positive temperature coefficient at rated current.

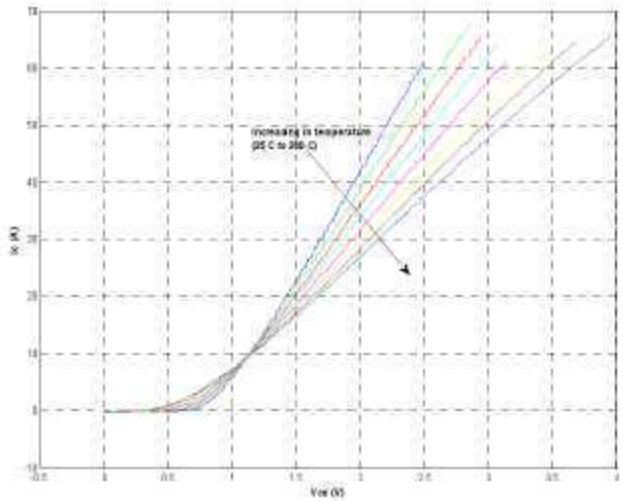


Fig. A.13. I-V characteristics of IGBT at different temperatures.

Only one leg of the IGBT module was utilized for the test. The other two legs were left 'floating.' An R-L load was connected across the upper IGBT. The upper IGBT was kept OFF by supplying -5V between the gate and the source (schematic below, Fig. A.14).

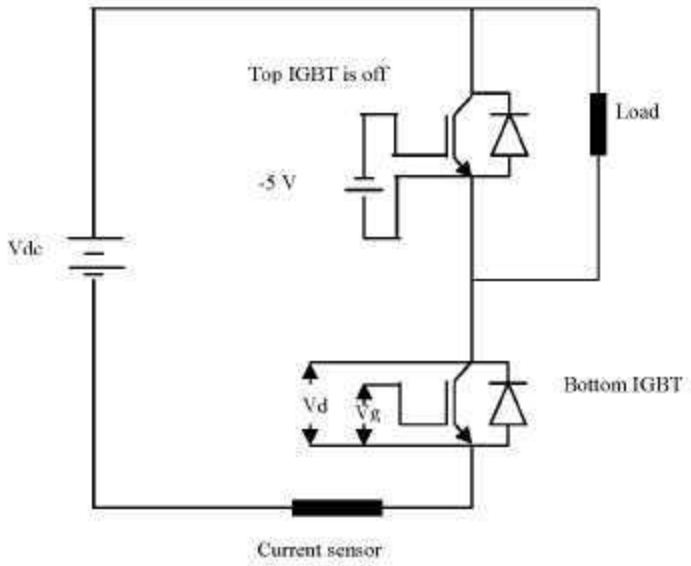


Fig. A.14. Schematic of the circuit.

A Fuji EXB840 chip was used as the gate driver. The lower IGBT was hard switched, no snubber was utilized. An Agilent 33250A waveform generator was used to generate the 5 kHz switching frequency with a duty cycle of 20%. A hot plate was used to vary the junction temperature of the IGBT. The IGBT module was mounted on a copper plate, which was fixed to the hot plate using thermal grease. The temperature of the hot plate was measured and fed back using a thermocouple to control the desired temperature (Fig. A.15).

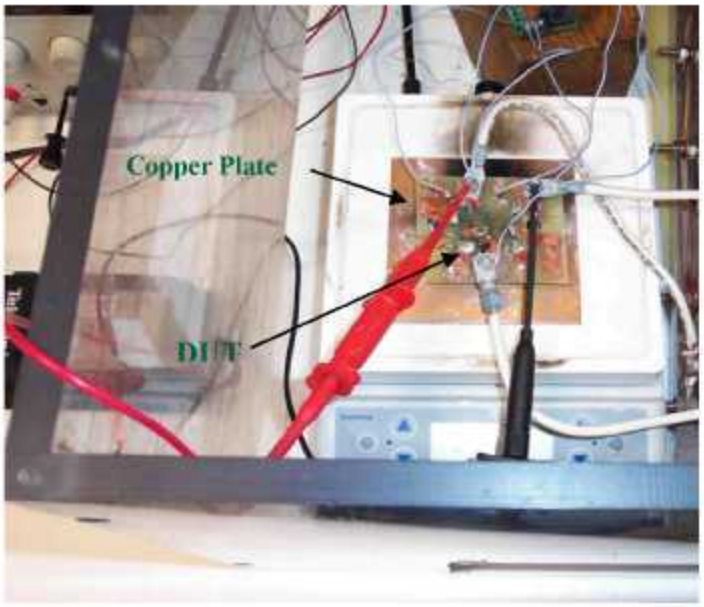


Fig. A.15. Test setup.

The device performed without a failure up to 175°C case temperature at different load conditions. The device was switched at 5 kHz, 250 V, 23 A (38 A peak during transient) current, 20% duty cycle, without any problems. The device was operated with different load conditions for at least 15 minutes for each data point. The IGBT failed at 250V, 16A operation at a case temperature of 200°C after operating for about 10 minutes. Similar steps were carried out on different legs of the module to confirm the failure. The IGBT failed consistently for operation at 250 V and 200°C at 23 A.

The device was subjected to continuous dc current tests to study the performance of the device close to the rated current. The voltage was increased in steps to obtain 5, 10, 15, 20, 25, and 30 A current levels. The tests were carried out at 50, 100, 150, 175, and 200°C case temperatures.

The device operated without any failure at 30 A (rated current), at 175°C. However, at 200°C case temperature the device worked well up to 25 A of current and failed at 30 A. The tests were repeated with another sample to confirm the failure point and the device failed again at 30 A. It can be concluded that the device is capable of successfully operating at 175°C without any failure. However, at a case temperature of 200°C the device fails at higher current levels both during the switching tests and the dc tests.

A.3.1.2 Fault current limiting tests of SiC JFETs

Most SiC power devices proposed for use in traction drives have positive temperature coefficients; this means that as the devices heat up, their resistance increases. In the case of a fault, the fault currents would heat up the device increasing the devices resistance. The increased resistance reduces the fault current; however, by the time the fault current is limited, damage can be done to the electrical drive system. Another way of limiting fault currents is to increase the device resistance by varying the gate voltage. For this task, ORNL studied the feasibility of including fault current limiting feedback to the gate driver of a SiC power switch and also studied the temperature response of SiC devices under short circuit conditions.

Several circuits were built for testing the short-circuit capability of SiC JFETs. The devices were tested for short-circuit current capability by applying short current pulses of different magnitudes. Figure A.16 shows the pulse current test waveforms at different current values for a (1200 V, 5 A) JFET. The current through the device was controlled by varying the pulse width and magnitude. The JFET exhibited self current limiting capability at zero gate voltage. The current saturated at 35 A for a (1200 V, 5 A) device. The current saturation value corresponds to the value in the device characteristic curve obtained at room temperature.

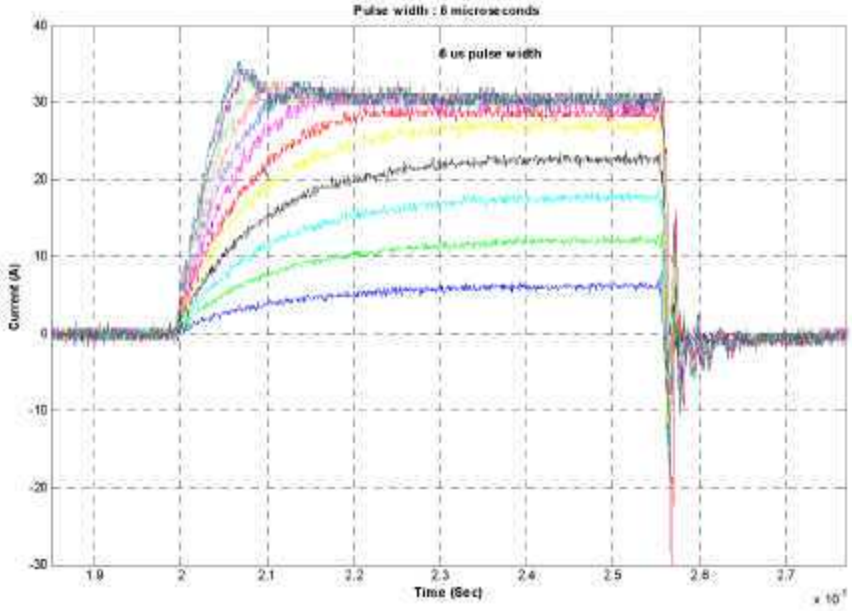


Fig. A.16. Short circuit pulse test waveforms of a SiC JFET.

The temperature response of the device was also studied by applying continuous dc current to the device to see the rate of change in resistance with temperature. The temperature response of the SiC JFET is shown in Fig. A.17. The tests showed that the positive temperature coefficient property of the device limited the current. However, as predicted, the time it takes for the device to limit the current is long because of the slow change in resistance with temperature. The time is on the order of several seconds and is too long for the device to withstand the short circuit current. It should be noted that the thermal time constant of the device package is also included in the total time.

To protect the device under fault conditions, a fault current limiting circuit is required. As mentioned earlier, the fault current can also be limited by varying the gate voltage. The variation in gate current with gate voltage can be obtained from the transfer characteristics. The gain (defined as change in current with change in gate voltage) of the JFET is an important parameter of the device for fault current limiting.

A fault current limiting circuit was developed and integrated into the gate driver circuit. Figure A.18 shows the schematic of the fault current detection and fault current limiting circuit under short circuit fault. The circuit was built using commercially available IC chips. The fault current detection is achieved by sensing the drain-source voltage across the device. The circuit has the blanking time capability which can be adjusted by varying the RC time constant between the gate turn-on signal and the detection signal. The blanking time prevents nuisance trips because of transient currents. The circuit has the flexibility to be adjusted for a particular on-state voltage drop between (0–7 V). The output stage of the gate driver

circuit is capable of handling 14 A of peak current. The circuit can be adapted for higher gate currents by implementing a complimentary transistor pair at the output stage of the gate driver.

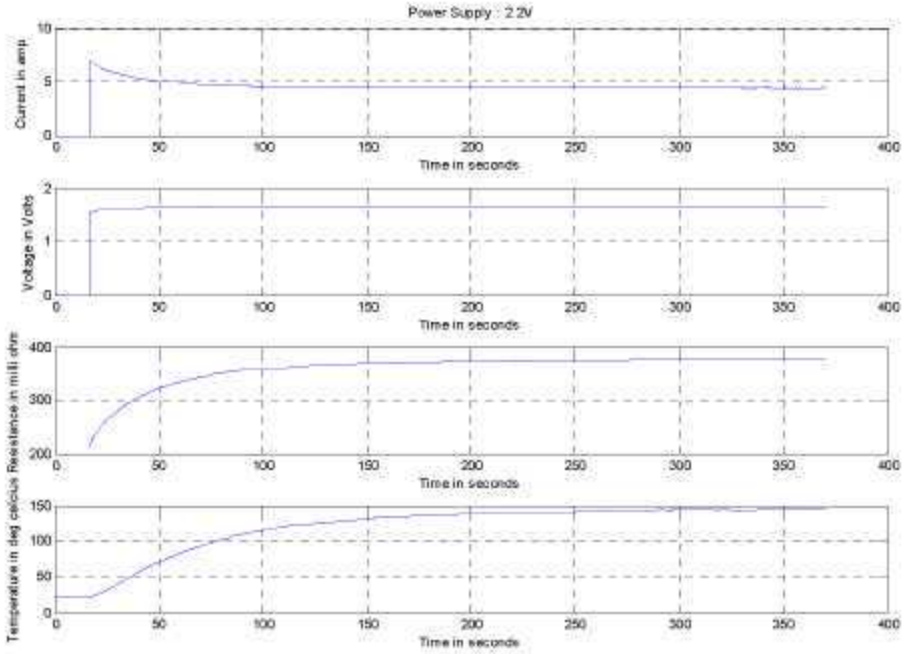


Fig. A.17. Temperature response profile of a SiC JFET.

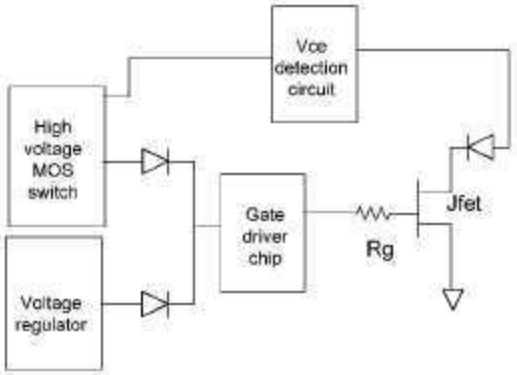
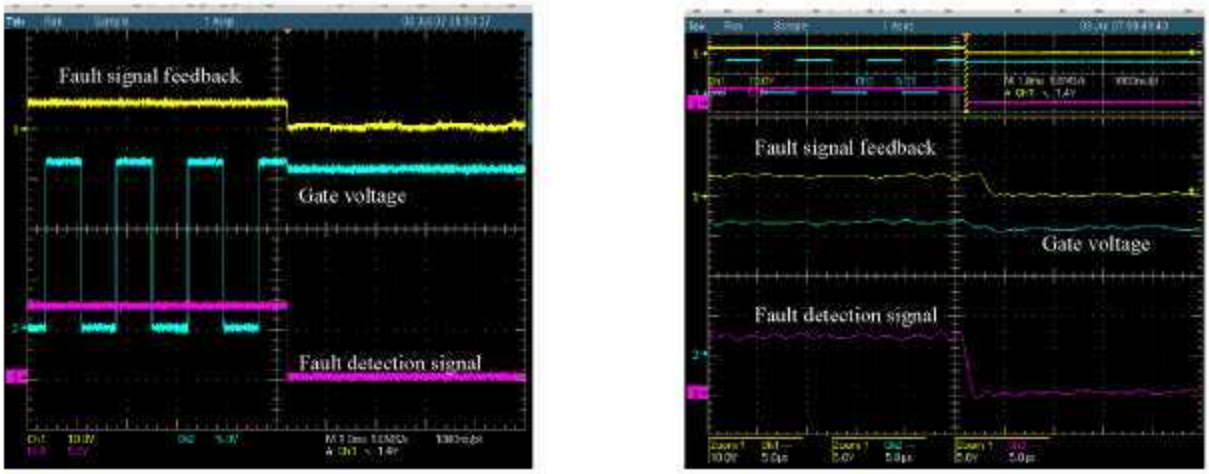


Fig. A.18. Schematic of the protection circuit for fault protection.

The waveforms in Fig. A.19 show the fault detection signal, the gate voltage waveform, and the fault signal feedback to the controller. The fault across the device is simulated using a preset voltage across the fault detection circuit, which in the actual device is the on-state voltage drop corresponding to the short circuit current. The gate voltage is clamped to a desired preset voltage as soon as the fault is detected. There is a delay between the fault detection signal and the fault signal output. However, the gate voltage starts to decrease even before the fault signal is active. This change in the gate voltage reduces the peak fault current immediately after the fault. The gate voltage is clamped to the preset voltage until the controller commands the turn-off the gate signal. The time needed for the gate voltage to be clamped is determined by the amount of time the device can withstand a short circuit. The protection circuit also has

the under voltage gate protection feature which will protect the device from damaging itself because of excessive losses.



(a) Normal view. **(b) Zoomed view.**

Fig. A.19. Test results of the protection circuit.

The circuit was tested with the device operating to verify the functionality of the circuit. The circuit was able to limit the current by changing the gate voltage. Figure A.20 shows the waveforms of gate voltage, drain current and, and drain voltage.

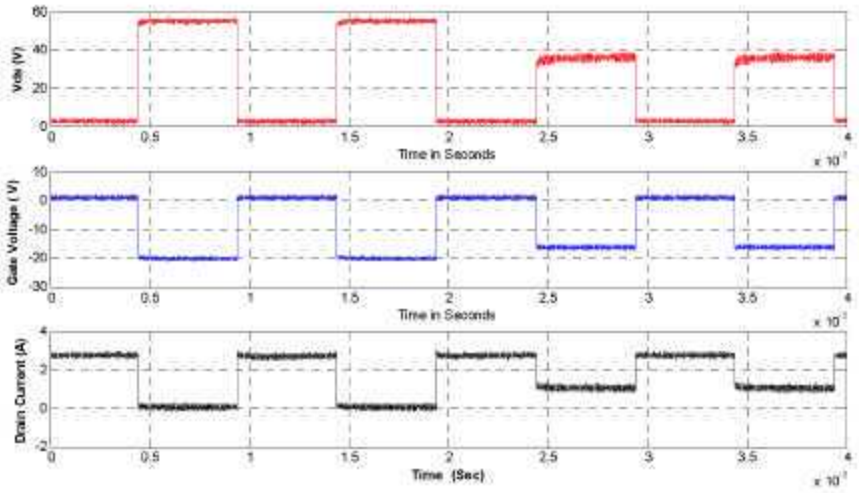


Fig. A.20. Gate voltage, drain voltage, and drain current waveforms of a SiC JFET.

A.3.1.3 Hybrid packaging

In order to take advantage of the high temperature operation capability of WBG devices, device packages that can withstand high temperatures are required. Various organizations are working towards high temperature packaging. Several high temperature packages which include discrete device packages to power modules have been reported in the past several years. However, even though the packages and devices can handle high temperatures, the low power electronics which drive the power devices are

limited to maximum temperatures of 200°C (silicon on insulator [SOI] based technology and Si based electronics are limited to 125°C). Additionally, SOI based electronics are expensive. High temperature (more than 200°C) electronics have been reported as being feasible; however, they have not been built or designed. It could be many years before a logic level high temperature transistor will be developed. This creates a void in the power module industry especially with the IPM products which include the electronics inside the module.

This proposed idea focuses on developing a hybrid package which includes high temperature WBG devices and low temperature Si electronics. The developed package will provide an intermediate solution before complete high temperature modules will be built. The innovative concept in this hybrid package is a thermal boundary layer separating the high temperature zone from the low temperature zone. This concept enables the use of low temperature electronics in close proximity with high temperature power devices in IPMs.

The SiC power device zone (high temperature) is allowed to operate at or below 300°C, and the Si control circuit zone (low temperature and low power) is kept at or below 125°C. The structure was modeled using the PRO-E CAD tool. To prove the concept, a feasibility study was done by modeling the package with different ambient conditions. The design concept was compared to a Si based IPM for physical sizing and heat flux requirements. The ambient temperature was fixed at 100°C, and it was assumed that fan driven convection cooling was used on the heat transfer surfaces of the modules. This ambient temperature allows a 25°C temperature gradient between the junction of the Si electronic devices and the ambient. The boundaries of the package were assumed to be insulated.

A comparison of the resulting module sizes is shown in Fig. A.21, indicating about a 75% reduction in volume when utilizing SiC for the power devices. The size reduction is mainly accomplished due to the reduced volume of the heatsink/fins, and reduced need for the typical heat spreading copper base in the conventional IPM. The results clearly indicate that the concept functions as expected.

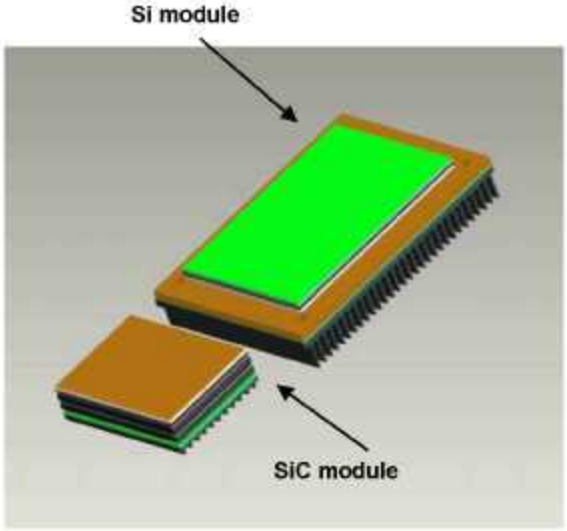


Fig. A.21. Comparison of sizes between Hybrid package and Si IPM.

A.3.1.4 PSAT traction drive model for a PHEV

PSAT HEV models use one integrated block that contains experimental data for the motor and the inverter called "motor controller". The power loss of the inverter can not be changed for different inverters since the data includes the motor's contribution. Therefore, new models were created to separate the motor and the inverter to be able to simulate all-Si and all-SiC inverters.

The inverter model computes the inverter average power loss based on device characteristics and motor performance, and uses an equivalent thermal circuit to estimate the rise of the device junction temperatures.

The motor model computes the ac current, voltage, and power factor of the motor and modulation index of PWM control that is used to calculate the losses in the inverter. The newly developed PSAT library block for the motor controller uses the above inverter and motor models to form a new motor controller model that uses the original block's inputs and outputs (Fig. A.22).

The model was simulated for an Urban Driving Scheme (UDDS) cycle with both Si-based and SiC-based inverters (assuming cooling conditions are the same). The results showed that the fuel economy is improved from 71.43–71.69 mpg (increased by 0.36%). The overall system efficiency is improved from 39.205–39.342% (increased by 0.35%).

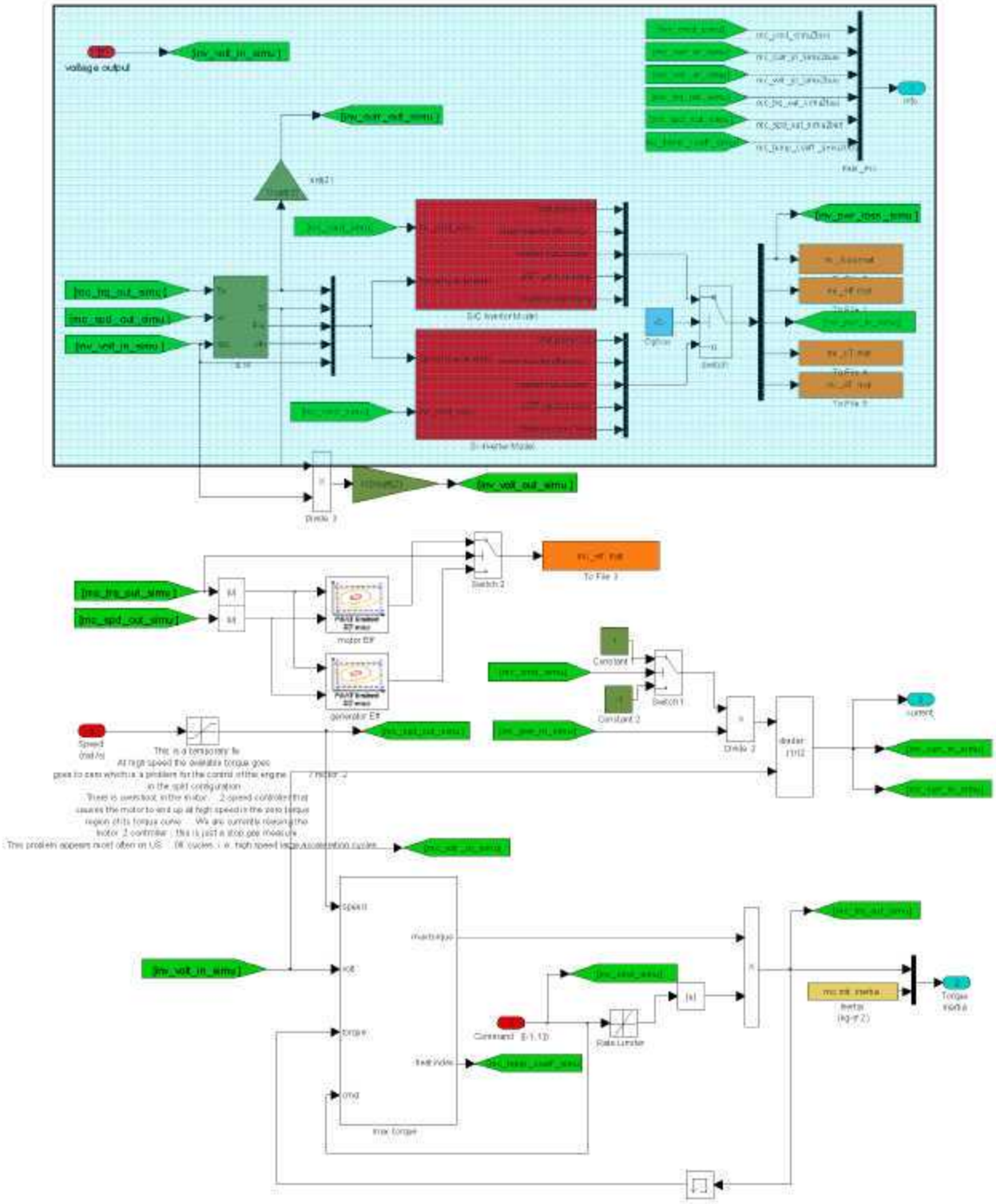


Fig. A.22. New motor controller model (the shaded portion shows the inverter models added to the block).

A.4 CONCLUSION

Several new devices (SiC Schottky diodes, JFET, and MOSFET) were acquired, tested and, modeled. A high temperature hybrid package was developed and modeled. The simulation results showed that the

package was feasible. An inverter loss model was successfully integrated into the drive train model in PSAT. The motor drive block in PSAT had one integrated unit. The motor drive in the drive train was split it into a motor and inverter block. Fault current limiting circuit for a SiC JFET was developed and tested.

A.5 FUTURE DIRECTION

- Acquire, test, and characterize newer technology WBG power devices.
- Study the conceptual changes to inverters/ converters and their packaging and thermal management designs to take advantage of WBG devices.

A.6 PUBLICATIONS

1. H. Zhang, L. M. Tolbert, B. Ozpineci, and M. Chinthavali, "A SiC-Based Converter as a Utility Interface for a Battery System," IEEE Industry Applications Society Annual Meeting, October 8–12, 2006, Tampa, Florida.
2. L. M. Tolbert, H. Zhang, M. Chinthavali, and B. Ozpineci, "SiC-based Power Converters for High Temperature Applications," European Conference on Silicon Carbide and Related Materials, September 3–7, 2006, Newcastle, UK.

A.7 REFERENCES

1. M. Chinthavali, B. Ozpineci, L. M. Tolbert, and A. S. Kashyap, *Wide Bandgap Semiconductors*, a technical report for the U.S. Department of Energy, UT-Battelle, LLC, Oak Ridge National Laboratory, ORNL/TM-2005-214, November 2005.

APPENDIX B

ORNL/TM-2007/046, *Power Module Investigation for High Temperature (175–200°C) Automotive Application*

U.S. Department of Energy
FreedomCAR and Vehicle Technologies, EE-2G
1000 Independence Avenue, S.W.
Washington, D.C. 20585-0121

FY 2007

POWER MODULATION INVESTIGATION FOR HIGH TEMPERATURE (175°C–200°C) AUTOMOTIVE APPLICATION

Prepared by:

Oak Ridge National Laboratory

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Submitted to:

Energy Efficiency and Renewable Energy
FreedomCAR and Vehicle Technologies
Vehicle Systems Team

Susan A. Rogers, Technology Development Manager

April 2007

OAK RIDGE
NATIONAL LABORATORY
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FOR THE DEPARTMENT OF ENERGY

ORNL/TM-2007/046

Engineering Science and Technology Division

POWER MODULATION INVESTIGATION FOR HIGH TEMPERATURE (175°C–200°C) AUTOMOTIVE APPLICATION

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University of Maryland

Publication Date: April 2007

Prepared by the
OAK RIDGE NATIONAL LABORATORY
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managed by
UT-BATTELLE, LLC
for the
U.S. DEPARTMENT OF ENERGY
Under contract DE-AC05-00OR22725

Final Report

Power Module Investigation for High Temperature (175°C-200°C) Automotive Application

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March 30, 2007

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Introduction

Hybrid Vehicle and Hybrid Vehicle Environment

Hybrid electric vehicles were re-introduced in the late 1990s after a century dominated by purely internal combustion powered engines[1]. Automotive players, such as GM, Ford, DaimlerChrysler, Honda, and Toyota, together with major energy producers, such as BP-Amoco, were the major force in the development of hybrid electric vehicles. Most notable was the development by Toyota of its Prius, which was launched in Japan in 1997 and worldwide in 2001. The shift to hybrids was driven by the fact that the sheer volume of vehicles on the road had begun to tax the ability of the environment to withstand the pollution of the internal combustion engine and the ability of the fossil fuel industry to produce a sufficient amount of refined gasoline. In addition, the number of vehicles was anticipated to rise exponentially with the increasing affluence of China and India.

Over the last fifteen years, major advances have been made in all the technologies essential to hybrid vehicle success, including batteries, motors, power control and conditioning electronics, regenerative braking, and power sources, including fuel cells. Current hybrid electric vehicles are gasoline internal combustion – electric motor hybrids. These hybrid electric vehicles range from micro-hybrids, where a stop/start system cuts the engine while the vehicle is stopped, and mild hybrids where the stop/start system is supplemented by regenerative braking and power assist, to full hybrids where the combustion motor is optimized for electric power production, and there is full electric drive and full regenerative braking. PSA Peugeot Citroen estimates the increased energy efficiency will range from 3-6% for the micro-hybrids to 15-25% for the full hybrids.[2] Gasoline-electric hybrids are preferred in US because they permit long distance travel with low emissions and high gasoline mileage, while still using the existing refueling infrastructure.

One of the most critical areas in which technology has been advancing has been the development of electronics that can operate in the high temperature environments present in hybrid vehicles. The temperatures under the hood for a gasoline-electric hybrid vehicle are comparable to those for traditional internal combustion engines. This is known to be a difficult environment with respect to commercial-grade electronics, as there are surface and ambient temperatures ranging from 125°C to 175°C. In addition, some hybrid drive electronics are placed in even harsher environments, such as on or near the brakes, where temperatures can reach 250°C. Furthermore, number of temperature cycles experienced by electronics in a hybrid vehicle is different from that experienced in a traditional vehicle. A traditional internal combustion vehicle will have the engine running for longer periods, whereas a mild or micro-hybrid engine will experience many more starts and stops.[3] This means that hybrid automotive electronics will undergo more cycles of a potential wider temperature cycle than standard automotive electronics, which in turn see temperature cycles of 2 to 3 times the magnitude of the ΔT = 50°C-75°C experienced by commercial-grade electronics.

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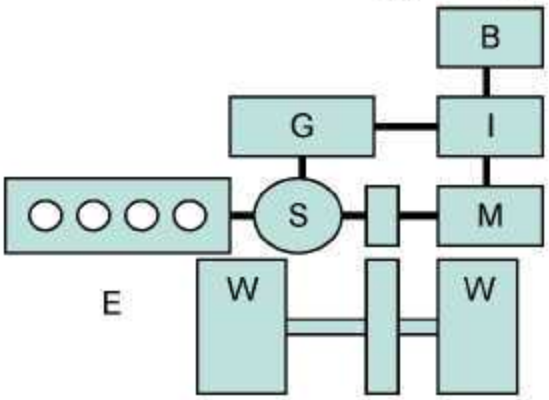
This study will discuss the effects of these harsh environments on the failure mechanisms and ultimate reliability of electronic systems developed for gasoline-electric hybrid vehicles. In addition, it will suggest technologies and components that can reasonably be expected to perform well in these environments. Finally, it will suggest areas where further research is needed or desirable. Areas for further research will be highlighted in bold, italic type.

It should be noted that the first area where further research is desirable is in developing a clearer understanding of the actual hybrid automotive electronics environment and how to simulate it through accelerated testing, thus:

Developing specific mission profiles and accelerated testing protocols for the underhood environment for hybrid cars, as has previously been done for gasoline-powered vehicles, is an important area for further study.

Elements of an inverter

Before discussing the high temperature performance and reliability of specific components and technologies, it is important to point out the elements of a typical hybrid automotive electronic system. The most advanced hybrids, such as the Toyota Prius, combine the best of both series and parallel configurations, as shown in Figure 1. When the vehicle is starting from rest, moving slowly, or going down a gradual slope - situations in which the engine does not operate efficiently – the engine is shut off. Only the electric motor powers the wheels by drawing power from the battery. Under constant-speed driving conditions, a fuel-efficient, 1.5 liter, four-cylinder engine delivers its output to both the generator and the wheels, through a planetary gear (power-split) device. The generator supplies power either to the electric wheel motors or to recharge the battery. During full throttle acceleration or under heavy load, the power from the battery is added to the power from the engine to boost the motor power driving the wheels. During deceleration or braking, the motor works as a generator to transform kinetic energy from the wheels into electrical energy to charge the battery.[4]



B = Battery (Fuel Cell)
I = Inverter
M = Motor
G = Generator
S = Power Splitter
E = Engine
W = Drive Wheels

Figure 1 A series/parallel hybrid system (Toyota THS)[4]

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An essential part of the hybrid drive system is the inverter, which converts DC power from the batteries/fuel cells or DC generator to AC power fed to the drive motor for the wheels. The inverter ensures the supply to the motors has a variable, controllable frequency. The inverter consists of a power semiconductor switching part that handles the main power flow through the inverter, and control circuitry that controls the power semiconductors and feeds back operating condition information to the main control center of the vehicle. The inverter in a hybrid vehicle is similar in its operation to the inverter part of a frequency converter widely used in industry.

Inverters are widely used in industry in a variety of applications, including variable frequency drives. A variable frequency drive controls the operating speed of an AC motor by using an inverter to control the frequency and voltage of the power supplied to the motor. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from mains AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters. It is these adjustable speed motor control inverters that are the main application for inverters in hybrid electric highway vehicles such as the Toyota Prius, as well as in some electric and diesel-electric locomotives. Various improvements in inverter technology are being developed specifically for electric vehicle applications.

There are a wide variety of inverter designs. In the simplest inverter circuit, DC power is connected to a transformer through the center tap of the primary winding. A switch is rapidly pulsed to allow current to flow back to the DC source following two alternate paths first through one end of the primary winding and then through the other. The alternation of the direction of current in the primary winding of the transformer produces alternating current (AC) in the secondary circuit. Power semiconductor devices, such as SCRs, Thyristors, GTOs, IGBTs, and transistors are used to do the switching.

The switch in the simple inverter described above produces a square voltage waveform as opposed to the sinusoidal waveform that is the usual waveform of an AC power supply. Using Fourier analysis, periodic waveforms, such as these square waveforms, are represented as the sum of an infinite series of sine waves. The sine wave that has the same frequency as the original waveform is called the fundamental component. The other sine waves included in the series, called *harmonics*, have frequencies that are integral multiples of the fundamental frequency. The quality of the inverter output waveform can be expressed by using the Fourier analysis data to calculate the total harmonic distortion (THD). The quality of output waveform that is needed from an inverter depends on the characteristics of the connected load. Some loads need a nearly perfect sine wave voltage supply in order to work properly. Other loads may work quite well with a square wave voltage.

The issue of waveform quality is addressed by using a variety of more advanced inverter designs with different power circuit topologies and control strategies. The approach selected depends on the way that the inverter is intended to be used. Capacitors and inductors can be used to filter the waveform. If the design includes a transformer,

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filtering can be applied to the primary or the secondary side of the transformer or to both sides. Low-pass filters are applied to allow the fundamental component of the waveform to pass to the output while limiting the passage of the harmonic components. If the inverter is designed to provide power at a fixed frequency, a resonant filter can be used. For an adjustable frequency inverter, the filter must be tuned to a frequency that is above the maximum fundamental frequency.

Since most loads contain inductance, feedback rectifiers or antiparallel diodes are often connected across each semiconductor switch to provide a path for the peak inductive load current when the semiconductor is turned off. The antiparallel diodes are somewhat similar to the *freewheeling diodes* used in AC/DC converter circuits.

Modulating, or regulating the width of a square-wave pulse, called pulse-width modulation (PWM), is often used as a method of regulating or adjusting an inverter's output voltage. When voltage control is not required, a fixed pulse width can be selected to reduce or eliminate selected harmonics. Harmonic elimination techniques are generally applied to the lowest harmonics because filtering is more effective at high frequencies than at low frequencies. *Multiple pulse-width* or *carrier based* PWM control schemes produce waveforms that are composed of many narrow pulses. The frequency represented by the number of narrow pulses per second is called the *switching frequency* or *carrier frequency*. These control schemes are often used in variable-frequency motor control inverters because they allow a wide range of output voltage and frequency adjustment while also improving the quality of the waveform.

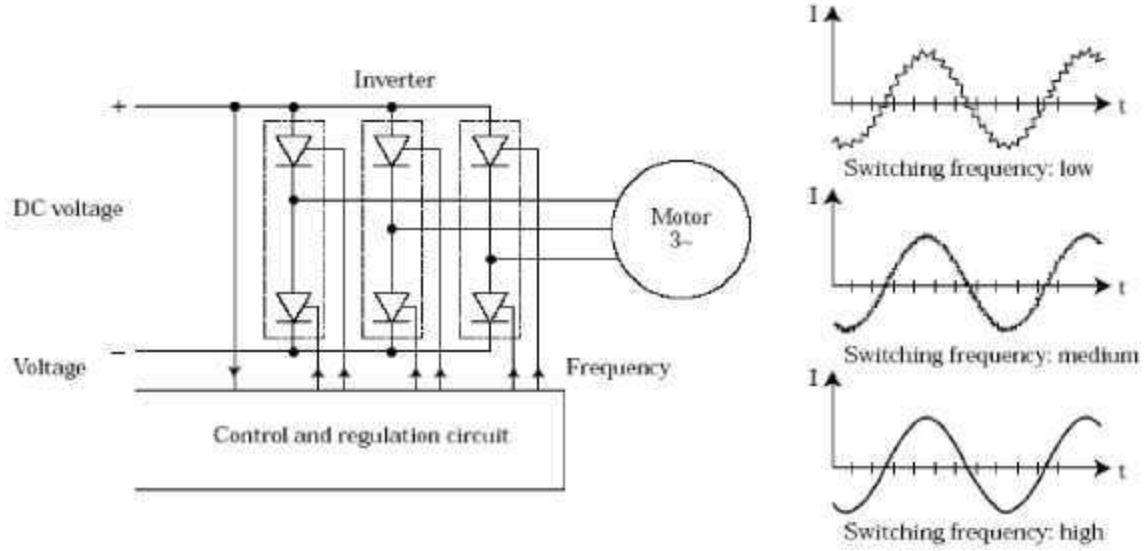

Figure 2 Inverter for variable or constant input voltage and output current dependent on the switching frequency. [5]

Three-phase inverters are used for variable-frequency drive applications and for high power applications such as HVDC power transmission. A basic three-phase inverter

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consists of three single-phase inverter switches each connected to one of the three load terminals. For the most basic control scheme, the operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform. This creates a line-to-line output waveform that has six steps. The six-step waveform has a zero-voltage step between the positive and negative sections of the square-wave such that the harmonics that are multiples of three are eliminated. When carrier-based PWM techniques are applied to six-step waveforms, the basic overall shape, or *envelope*, of the waveform is retained so that the 3rd harmonic and its multiples are cancelled.

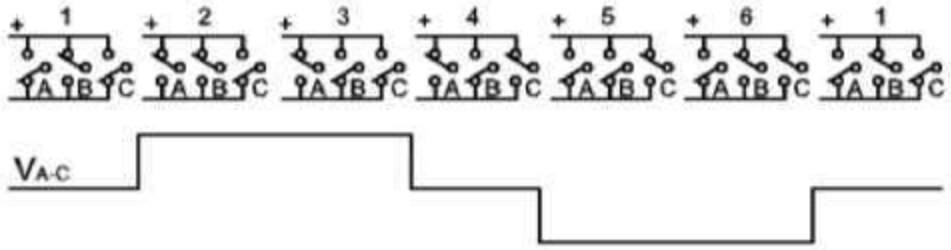

Figure 3 Three-phase inverter switching circuit showing six-step switching sequence. [5]

To construct inverters with higher power ratings, two six-step three-phase inverters can be connected in parallel for a higher current rating or in series for a higher voltage rating. Although inverters are usually combined for the purpose of achieving increased voltage or current ratings, the quality of the waveform is improved as well.

The typical three-phase inverter has 6 power semiconductors that are turned on and off by signals generated by the control circuit.[5] The inverter switching frequency is a balancing act as high frequency switching leads to high peak voltages and motor winding heating. On the other hand low switching frequency can lead to high acoustic noise. Power semiconductor switches fall into the following four main categories:

- Thyristors
- Bipolar Transistors
- Unipolar Transistor (MOSFET)
- Insulated-Gate-Bipolar Transistor (IGBT)

Bipolar transistors and Thyristors can pass large quantities of current with low on-state losses. MOSFETs provide fast switching speed with low switching losses. Today, IGBT transistors are the most widely used power switches as they combine the fast and low loss switching properties of the MOSFET with the high current carrying capability and low on-state losses of bipolar transistors and thyristors.[5] This permits them to control near thyristor levels of power at near MOSFETs switching frequencies as shown in figure 4.

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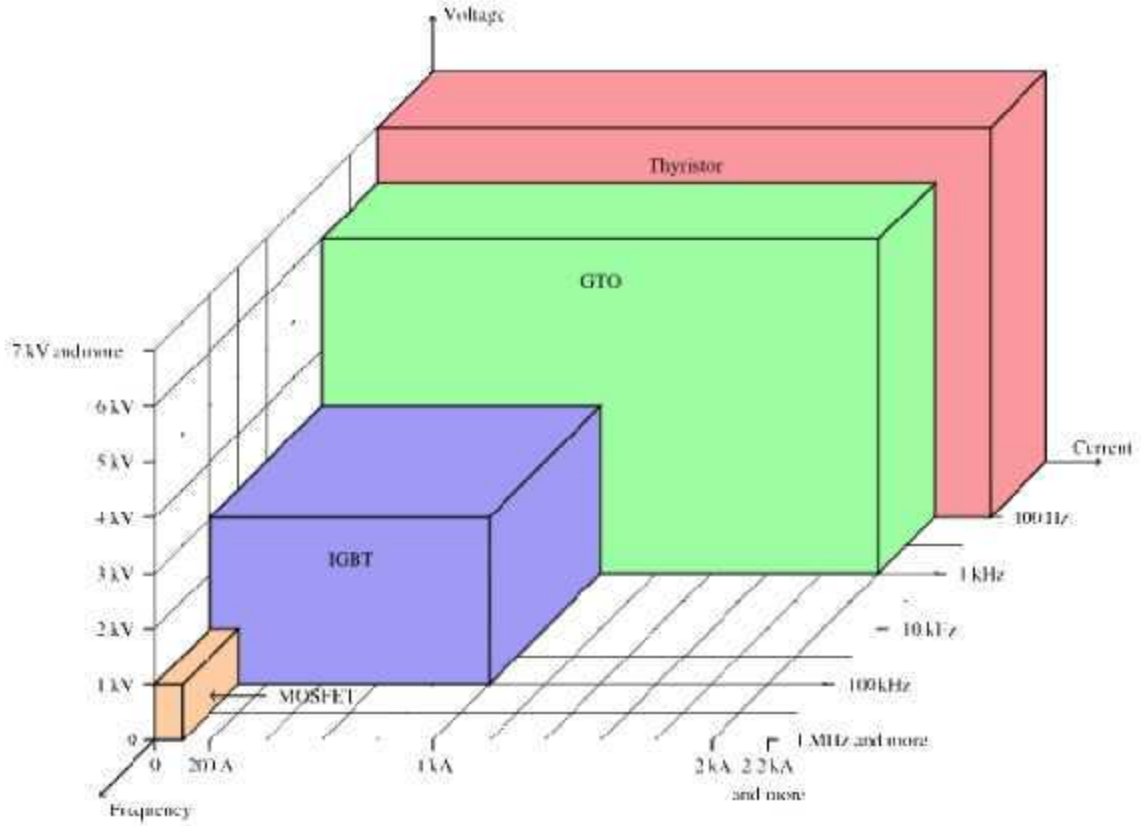

Figure 4 **Power and frequency range of power transistors.[6]**

Typical components for hybrid inverters make use of diodes and transistors rated for use in the 100-1200 VDC range and up to 100A, as used in frequency converters. One of the key factors in designing the circuitry for inverter drives is to keep the currents in the system as low as possible to reduce the conductive losses in the system.[7]

Silicon-based diodes and MOSFETs are available for operation over temperature ranges from -55°C to 150°C and Silicon-based IGBTs are available for operation over temperature ranges from -55°C to 175°C from a wide variety of manufacturers including ABB Semiconductor, Advanced Power Technology, Infineon, International Rectifier, IXYS, ON Semiconductor, Powerex, and others. These devices need to be capable of high temperature operation not only because of the 125°C to 175°C environment in which they are placed but also because of additional increases in temperature resulting from self-heating (i.e. Joule heating) due to power losses in the component. This is one of the major reasons why silicon carbide based power devices are now coming into widespread commercial use as well, with diodes and JFETs available for operation at temperatures to 300°C from SiCED, SemiSouth Laboratories, and Cree. SiC devices also have a number of other advantages over silicon devices for power applications besides the ability to operate reliably at higher temperatures. These include higher reverse bias blocking voltage owing to a higher dielectric breakdown field strength, faster switching

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speed because of a higher saturated electron drift velocity, and better heat dissipation due to greater thermal conductivity.

Further effort is needed in the development of SiC MOSFETs and IGBTs and their associated packaging.

In addition to the power switches, the inverter also interfaces with control circuitry, the task of which is to turn the power switches on and off according to the chosen strategy of modulation, typically PWM. It is also the task of the control circuitry to forward input from the drive train to the main control of the car. The control circuitry consists of small signal (i.e. low voltage) semiconductors. These devices handle smaller power levels than the power switches and therefore have little self heating. However, they are often located in close proximity to the power devices or other heat dissipating components such as the brakes or engine top. Therefore, the control circuitry experiences the same harsh under-the-hood environment as the power semiconductors.

Component Issues

Semiconductors

The most fundamental limitation to the use of any semiconductor at elevated temperatures is the increasing density of intrinsic carriers, which is shown in Figure 5[8]. Intrinsic carriers arise from the thermal generation of electron-hole pairs across the entire bandgap, and they are the only carriers in a pure (undoped) semiconductor material. Semiconductor devices are based on the interaction between areas of the semiconductor that are donor doped (n-type), and those which are acceptor doped (p-type). As the temperature is increased, eventually the intrinsic carrier concentration reaches the same order of magnitude as the doping concentration. At this point, semiconductor devices become inoperable as the ability to differentiate between n and p regions is lost. One way to counteract this effect is to increase the doping density. However this has the effect of decreasing the junction width and thus decreasing the reverse bias needed for junction breakdown.

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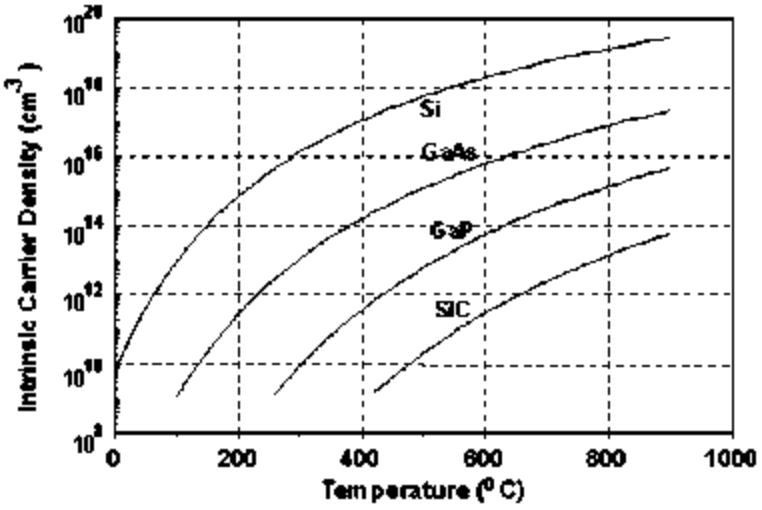

Figure 5 Effect of temperature on the intrinsic carrier concentration *[8].*

The higher intrinsic carrier concentration produces a number of adverse effects in silicon devices including increased reverse bias junction leakage current in p-n diodes, altered gain in bipolar transistors, shifts in the threshold voltage of MOSFETs, and latch-up in MOSFETs as a result of increased leakage across the p-n isolation junctions.

The increase in leakage current with increasing intrinsic carrier concentration was observed experimentally by Bromstead [9]. Bromstead found that I_{CE} leakage current in bipolar devices increases 8% /K. This increase in leakage current subsequently resulted in increased gain and decreased efficiency in bipolar devices.

It is this increase in leakage current which limits the operating temperature of power diodes, bipolar junction transistors, IGBTs, and thyristors. Silicon devices typically have a safe operating area that permits operation at junction temperatures to 175°C. This equates to ambient temperatures of up to 175°C with derating of current as the ambient temperature rises, from full current at 125°C to zero current at 175°C. Derating lessens the power generation and therefore the self-heating in the device. For temperatures greater than this, much research is ongoing into the development and use of SiC diodes, and JFETs. These devices take advantage of the wider bandgap in SiC and its corresponding smaller intrinsic carrier concentration to reduce leakage levels. Working devices have been made that can be operated reliably at temperatures to 400°C.

With the elimination of the micropipe problem, limitations to SiC power devices now rest with screw dislocation assisted reverse breakdown, ohmic contact issues, interconnection and packaging.

The effects of increased temperature on MOSFET devices include decreasing the threshold voltage. The threshold voltage decrease (dV_T/dT) in a typical n-MOSFET is 2mV/K to 6mV/K depending on the thickness of the gate oxide and the doping density [10]. The reduction in threshold voltage lessens the immunity of the circuit to noise,

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thereby making it more likely for the device to turn on solely on the basis of a noise pulse, rather than an actual signal. Therefore, while MOSFET transistors can be used as switches at high temperatures, designs must account for reduced noise margins.

Low field carrier mobility is also degraded at elevated temperatures [11], which lowers the transconductance in MOSFETs in the linear regime below saturation. This reduces analog device gain and can slow digital device switching speeds. High temperatures can slow switching speeds even further by increasing the resistance of the metallization traces, thereby increasing the time delay due to the on-chip interconnections. This often has a greater effect than the decrease in the low field mobility.

For this reason, it is necessary to slow the clock speed of circuits containing microprocessors if they are to be used at elevated temperatures. Linear and analog devices can be used in a more straightforward manner at high temperatures, but the change in their parameters must be taken into account in the design.

Power MOSFETs, like small-signal MOSFETs, are susceptible to changes in threshold voltage, noise immunity and switching speed at high temperatures. For these reasons, typical silicon power MOSFETs are limited to temperatures less than 175°C with appropriate current derating as discussed for the bipolar devices. SiC power MOSFETs have been made that can operate at junction temperatures greater than 175°C, however, to date, the poor quality of the $SiC-SiO_2$ interface has produced high levels of trapping and leakage, and limited their maximum junction temperature to below 250°C.

It is the adverse effect of leakage current on CMOS devices, however, that is perhaps of the most importance to small signal controls, such as are used in the engine control, braking control, and HEV control computers. Leakage current, first and foremost, increases the susceptibility of CMOS devices to latch-up. Latch-up refers to the unintentional turning on of the parasitic SCR formed by the four layer $p^+np^-n^-$ structure between the ground and the power rail, which exists in every p-substrate n-well CMOS device. To initiate and maintain this state, a minimum value of current, called the trigger current (I_{trg}), must initially be supplied to the base of one of the transistors, and a minimum value of current, called the holding current, must continue to flow through the device. [12].

Latch-up can have devastating consequences as it shorts the power rail to ground in the particular device in which it is observed, and it can generate sufficient heat to cause other devices and/or the entire integrated circuit to fail as well. The following four factors lead to increased latch-up susceptibility at increased temperature:

- Lower values of trigger and holding currents at higher temperatures
- Higher leakage currents at higher temperatures which can serve to trigger latch-up
- Higher values of well and substrate resistances at higher temperature, causing a greater voltage drop which facilitates the feed-forward current loop.
- Increased bipolar current gains (b_n and b_p) and common base current gains (a_n and a_p) at higher temperatures which facilitate the feed-forward current loop.

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Almost all CMOS devices succumb to latch-up at high temperatures. The temperature at which this occurs depends on the geometry and technology of the device with bulk devices beginning to exhibit latch-up at temperatures as low as 125°C, and epitaxial layer devices exhibiting latch-up at temperatures above 200°C. The most cost-effective technology providing immunity to latch-up at temperatures up to 300°C is silicon-on-insulator (SOI). Silicon-on-insulator technology uses an insulating layer such as SiO_2 to partially isolate the n-MOS and p-MOS devices, instead of relying solely on reverse biased p-n junctions. By placing the devices in epitaxial silicon on SiO_2, the junction area between the devices is reduced [13, 14]. As the leakage current across a silicon n+p junction is proportional to the junction area, a decrease in junction area significantly lowers the leakage current, ensuring latch-up immunity [13]. This decrease in leakage current is shown in Figure 6. Honeywell currently markets a line of SOI devices for high temperature and radiation-hard applications that can be used reliably for up to 5 years at 225°C, and for short periods up to 300°C.

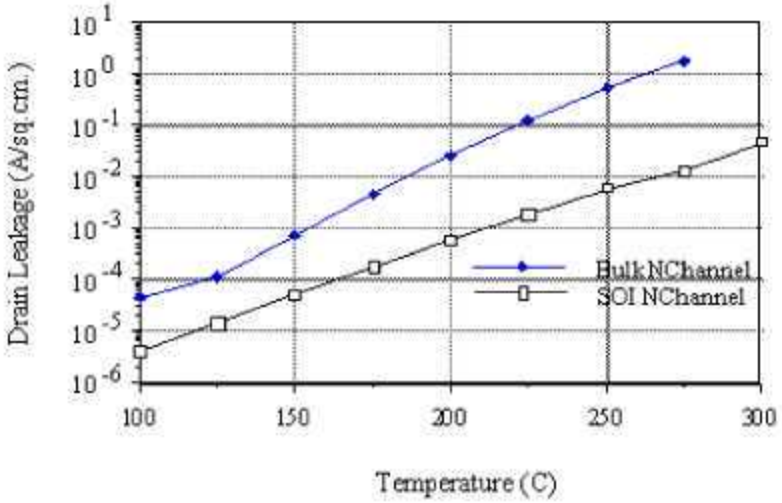

Figure 6 **Temperature dependence of leakage current in bulk and SOI CMOS [13]**

The effects described above limit the maximum ambient use temperature of junction isolated small-signal silicon devices to 175°C -200°C.[15] However, the performance of silicon devices at the highest levels of integration may begin to degrade at even lower temperatures. 200°C operation depends on circuit design tailored for high temperature applications, which includes scaling the gate in channel length to improve the transconductance, while increasing the channel width to inhibit latch-up. Other high temperature design rules include providing adequate spacing, aligning transistors source to source, and using guard structures [16].

While understanding parameter shifts in silicon devices is critical to using them at elevated temperatures, it is also important to address the more insidious reliability concerns. Time dependent dielectric breakdown of the gate oxide in a MOSFET is accelerated at elevated temperatures [17], and can cause failure of the device in several hours at 200°C and 8 MV/cm field strength. However, decreasing the field strength to 2 MV/cm, removes this concern [10]. The appropriate choice of oxide thickness can thus reduce the electric field sufficiently to eliminate high temperature concerns. However,

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with today's extremely small channels and correspondingly scaled effective oxide thicknesses of less than 2 nm, it becomes increasingly difficult to limit the occurrence of this failure mechanism at elevated temperatures. The decreasing gate voltage (from 5V → 2.5 V or less) does help somewhat to mitigate this concern.

Similar tradeoffs must be addressed for electromigration. Aluminum, the primary metallization for silicon systems, is resistant to electromigration in highly integrated devices at temperatures below 150°C. By designing for high temperature use, which includes increasing the cross-section of the lines and using lower current densities, concerns can be avoided up to 250°C [9]. However, new microprocessors contain copper metallization, which, when processed correctly with good adhesion to the underlying dielectric, promises greater electromigration resistance and lower resistivity. However, poor adhesion of the copper to the underlying dielectric can actually lower electromigration resistance over that seen in aluminum metallization.

Furthermore, high temperature ohmic contacts to SiC and the resistance of the gold-based metallizations to electromigration are topics requiring additional study.

While the above discussion provides absolute limits to the use of silicon devices and other device technologies, most small-signal semiconductor devices in widespread circulation today are specified for use in the "commercial" 0 to 70°C, and to a lesser extent in the "industrial" -40 to 85°C, operating temperature range, thus satisfying the demands of the computer, telecommunications, and consumer electronics and their markets. There is, however, demand for parts rated beyond the "industrial" temperature range, primarily from the aerospace, military, oil and gas exploration, and automotive industries. However, the demand is often not large enough to attract and retain the interest of major semiconductor part manufacturers in producing extended temperature range parts.[18] Nevertheless, a method has been suggested to enable the use of commercial-off-the-shelf control circuitry semiconductor devices at an elevated temperature condition, such as the automotive underhood environment. This is to apply uprating methodologies to packages specified to more common temperature ranges. Uprating may permit the use in harsher environments of components that incorporate the latest technological advancements in the electronics industry in terms of performance, cost, size, and packaging styles.

The discussion of uprating in this document is not meant to be an endorsement of this procedure and is only submitted for educational purposes.

Electronic parts are currently being used outside their specifications in many applications and industry sectors [19, 20], such as oil and gas exploration and recovery, home appliances and commercial, avionics and defense electronics among others. Uprating has been successfully implemented in several government and air transport products (e.g., avionics for Boeing 777) since 1994 [21]. Even the Federal Aviation Authority (FAA) of the United States conditionally accepts the use of parts outside the manufacturer's specifications. It states that "If the declared installation temperature environment for the EEC (Electrical and Electronic Components) is greater than that of the electronic parts

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specified in the engine type design, the applicant should substantiate that the proposed extended range of the specified components is suitable for the application."

On the other hand, some electronic part manufacturers are critical of the use of parts outside their ratings. National Semiconductor, for example, states that using parts in applications or environments for which they were not intended can lead to part or system failure. National Semiconductor strongly recommends that its products be used only within the electrical and environmental limits published in their respective datasheets [22]. Intel has also stated that it will not accept any legal responsibility for failures that occur due to the deliberate misuse of its products, including any damages resulting from the practice of uprating. Similarly, there are warnings from other manufacturers and trade associations such as Analog Devices [23], Xilinx[24], Texas Instruments [25, 26], and Semiconductor Industry Association (SIA)[27].

Parts are uprateable for temperature because part manufacturers generally provide a margin between the recommended operating temperature specification of a part and the actual temperature range over which the part will operate. This margin helps maximize part yields, reduce or eliminate outgoing tests and optimize sample testing and statistical process control (SPC). Sometimes this margin can be exploited, and thus the part can be uprated. For example, Motorola notes [28] that, "There is no manufacturing difference between PEMs (plastic encapsulated microcircuits) certified from 0 to 70°C and those certified from -55 to 125°C. The same devices, the same interconnects, and the same encapsulants are used. The only difference is the temperature at which the final electrical testing is done." In fact, many electronic parts manufacturers have used the same die for various "temperature grades" of parts (commercial, industrial, automotive, and military). For example, Intel[29] stated in their military product data book: "there is no distinction between commercial product and military product in the wafer fabrication process. Thus, in this most important part of the VLSI manufacturing process, Intel's military products have the advantages of stability and control which derive from the larger volumes produced for commercial market. In the assembly, test and finish operations, Intel's military product flow differs slightly from the commercial process flow, mainly in additional inspection, test and finish operations."

The best way to see if a part is uprateable, is to obtain the simulation and characterization data from the part manufacturers. The data include product objective specifications, product and packaging roadmaps, device electrical simulation models, and temperature characterization data. Depending on the part manufacturer, some of these data are available freely, while other may be available upon request or in some cases by signing a non-disclosure agreement.

The effects of temperature (and other factors such as voltage and frequency) on different electrical parameters can be estimated using models available from part manufacturers. Often the device electrical simulation models are made available to the public, although the models are often 'sanitized' so that any proprietary information is masked [30]. Simulation models of devices can be used to calculate the effects of temperature variation on device parameters (e.g., the BSIM3 model for short channel MOSFETs) [31]. Device

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simulations therefore can be used to estimate if the part will be uprateable, and what parameter changes may be expected at application operating conditions.

There are three types of uprating (viz. parameter conformance, parameter re-characterization, and stress balancing). Parameter conformance is a process of uprating in which the part is tested to assess if its functionality and electrical parameters meet the manufacturer's recommended operating conditions over the target temperature range. The tests are of a "go/no-go" type, and are generally performed at the upper and lower ends of the target application conditions. A margin may be added to the test, either in a range wider than the target application conditions or in tighter electrical parameter limits for the test. The electrical parameter specifications in the datasheet are not modified by this method.

Parameter re-characterization is a process of uprating in which the part functionality is assessed and the electrical parameters are characterized over the target application conditions, leading to a possible re-specification of the manufacturer-specified datasheet parameter limits. The parameter re-characterization method of uprating seeks to mimic the part manufacturer's characterization process. Electrical testing is followed by data analysis and margin estimation.

Stress balancing is a process of thermal uprating in which at least one of the part's electrical parameters is kept below its maximum allowable limit to reduce heat generation, thereby allowing operation at a higher ambient temperature than that specified by the semiconductor part manufacturer[32]. The process assesses the possibility that the application may not need to use the full performance capability of the device, and that a power versus operating temperature trade-off for the part may be possible.

Uprating deals with performance over a wider temperature range not reliability, Reliability is the ability of a part to perform within specified performance limits, for a specified period of time, under the life cycle application conditions. Reliability assessment MUST be performed independently of the performance assessment step (where uprating may be carried out), because the recommended operating conditions that are stated in the part datasheet, relate only to the electrical parameter limits. Generally, the manufacturing, qualification and reliability monitoring data are used to help in the reliability assessment[33].

In general, the manufacturer's part qualification process is not based on the part's recommended operating conditions but rather on accelerated reliability testing methods[34]. In other words, part operating temperature ratings are set for performance reasons as opposed to reliability reasons. The limits for reliable operation of parts are designated by the absolute maximum ratings (most often wider than the recommended operating conditions). In fact, there have been several studies where the reliability of parts has been tested beyond their manufacturer-specified recommended operating temperature limits and the reliability demonstrated for the application [32, 35-38]. There have also been studies where the reliability of parts has been tested beyond their absolute maximum ratings and the reliability has been demonstrated for the application [39]. The cause of uprating does not necessarily compromise reliability [40, 41].

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Nevertheless, the uprating assessment of a part only determines the electrical functional capability of parts in their target application conditions. This determines whether a part "can work" in a given environment. However, to determine if a part "won't fail" in the application environment, the reliability of the part needs to be determined for the application. As temperature often accelerates failure in electronic components, and since the manufacturer has no responsibility to ensure reliability outside the recommended temperature range of operation, it is the responsibility of the part user to establish part reliability over a wider temperature range, before using the device outside the recommended temperature range. The methods of determination of reliability can vary and may include assessment of manufacturers' qualification test results, additional tests performed by the equipment manufacturers and virtual qualification.

Capacitors

One of the most difficult technological barriers to the development of high temperature electronic systems is the creation of compact, thermally stable, high energy density capacitors. Fundamental properties of traditional, perovskite ceramic, dielectric materials dictate that stability of capacitance with respect to temperature and voltage must be sacrificed to achieve large values of the dielectric constant.

	Manufacturer	Voltage	Performance Range	Temp Range
Ceramic	KEMET	100 - 200 Vdc	16 pF - 0.1uF	+ 200 C
		101 - 200 Vdc	1000 pF - 1.0 uF	+ 200 C
		50, 100, 150 Vdc	1.0 pF - 0.12 uF	+125 C
		50, 100, 150 Vdc	100 pF - 6.8 uF	+125 C
	Johanson	50, 100, 200 Vdc	470 pF - 0.075 uF	-55 - 200 C
		50, 100, 200 Vdc	3900 pF - 1 uF	-55 - 200 C
	Syfer	25, 50, 100, 200 Vdc	1 nF - 1.80 uF	-55 - 150 C
	Novacap	25, 50, 100, 250, 500 Vdc	120 pF - 18 uF	-55 - 200 C
		25, 50, 100, 250, 500 Vdc	5600 pF - 15 uF	-55 - 150 C
		25, 50, 100, 250, 500, 1000, 2000, 3000, 4000 Vdc	47 pF - 390 nF	-55 - 200 C
	AVX	16,25,48 V	270 pF to 0.47 uF	-55 to 150 C
	TDK	25, 50, 100 Vdc	150 pF - 4.7 uF	-55 - 150 C
	Murata	50 Vdc	2700 pF - 0.022 uF	-55 - 150 C
		50 Vdc	0.047 uF - 0.33 uF	-55 - 150 C
		16, 50 Vdc	0.22 uF - 2.2 uF	-55 - 150 C
Film	AVX	25 - 250 Vdc	1 nF - 33 nF	-55 - 140 C
	Evox Rifa	50, 100, 250, 400 Vdc	1 nF - 3.3 uF	-55 - 150 C
		50, 100, 250, 400 Vdc	1 nF - 22 uF	-55 - 150 C
		50, 100, 250, 400 Vdc	1 nF - 0.56 uF	-55 - 150 C
		100, 250, 400, 630 Vdc	470 pF - 0.68 uF	-55 - 150 C
	Custom Electronics	100, 200, 400, 600 Vdc	Call for range	< 200 C
		200, 400, 600 Vdc	Call for range	< 200 C

Figure 7 Typical ratings for capacitors for extreme temperature environments.

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As seen from Figure 7, only a few capacitors are available for the hybrid automotive temperature environment.

Low dielectric constant materials ($\varepsilon_r < 50$), which are used in temperature compensating capacitors, such as C0G or NP0, are highly stable with respect to temperature, have a predictable temperature coefficient of capacitance, and exhibit few adverse effects of aging. However, the volumetric energy density is so low that it takes hundreds of very thin layers to produce even a 1 μF capacitor. Higher dielectric constant titanates which are used to provide higher energy density for general purpose ceramic capacitors, such as X7R, exhibit wide variations in dielectric constant with increases in temperature, including a rapid drop in dielectric constant above 150°C. In fact, the capacitance of X7R at 200°C can easily be less than 60% of the room temperature value. In addition, the leakage currents in these titanate materials become unacceptably high at elevated temperatures, making it more difficult for the capacitor to hold a charge, and the increased dissipation factors can lead to thermal runaway. For the regime 150°C to 300°C, the preferred method is to eliminate as many capacitors as possible from the design, and then to use stacks of highly thermally stable NP0 dielectrics to achieve the desired capacitance. Glass-K capacitors have also shown promise in this temperature range.[42] Much materials research is currently ongoing to push out this power density/temperature stability tradeoff. One example of this is the use of different heating rates and atmospheres in the manufacture of PLZT ceramics to create highly volumetrically-efficient capacitor dielectrics with long-term stability at high operating temperature (T > 200°C) and moderate applied voltage [43]. Another is the development of a new family of relaxor ferroelectric materials based on $BiMeO_3$-PT, where Me^{+3} is a metal ion that can be Sc^{-3}, Yb^{-3}, Y^{+3}, Fe^{+3}, or others. These materials have dielectric constants of more than 10,000 and dissipation factors less than 2% over a wide temperature range with maximum operating temperatures ranging from 300°C to as high as 600°C. These relaxors have been used to create capacitors with volumetric efficiencies greater than 1.4 $\mu F/cm^3$ at 300°C [44]. Capacitors made with these new dielectric materials are now commercially available from TRS Ceramics.

As for capacitors based on metallized polymer films, those polymer dielectrics that are mechanically and electrically stable to the highest temperatures, such as polyimide and teflon, are also the films which have the lowest dielectric constants and are the most difficult to manufacture in very thin layers. For many years, polyester film dielectrics have been the mainstay of the energy storage capacitor industry. However, polyester dielectric capacitors have been viewed as weak candidates for high temperature applications exceeding 150°C because of their relatively low glass transition temperatures, although some previously accepted limitations are likely to be more related to packaging and manufacturing than to the basic properties of the polyester film [45].

For applications at temperatures to 200°C, a number of different dielectrics have been examined, including Nomex 410 and 418 aramid papers; Voltex 450 aramid paper; polybenzimidazole (PBI), a linear thermoplastic supplied by Hoescht Celanese [46-48]; FPE Polyimide [49], Kapton [50], Polyimide (PI), Perfluoroalkoxy (PFA) resin, and Polyparaxylene (PPX) [51]. Of these, the best candidates were the FPE polyimide, which exhibited stable capacitance and dissipation factor up to 225°C for up to 500 hours, and

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PFA, which combined stable mechanical and thermal properties with a low dielectric loss and a relative permittivity which remained within ± 10% of the room temperature value to 200°C.

Despite these investigations, clearly the outstanding polymer candidate for 200°C capacitors is still PTFE because of its stability with respect to temperature. For 1.0 mF components, aged in an air ambient for 2000 hours (12 weeks) at 200°C, and then brought to room temperature, teflon capacitors exhibited very little change in capacitance at 50 khZ and only a gradual decrease in capacitance at 20 kHz to 98% of the original value. The dissipation factor of the capacitors tested increased slightly and gradually, at 50 Hz, throughout the duration of the testing.[52, 53] Further information can be found in review articles on polymer film capacitors [42, 54].

Other Passives

Inductors are often the largest and heaviest components in power electronic systems [55]. Therefore, efforts to miniaturize inverters for use in hybrid electric automotive applications must necessarily consider improvements in these devices. Furthermore, these applications will require that these components operate at elevated temperatures. Advancements in magnetic materials for power electronics are needed to permit both reduction in the size and weight of inductive components and facilitate their use at elevated temperatures.

The desired technical properties for soft magnetic materials are high permeability, low hysteresis loss, low eddy current loss, large saturation and remnant magnetization, and high Curie temperatures. Permeability describes the magnetic induction, B, produced by a given applied field, H. Hysteresis loss is the energy consumed (and dissipated as heat) in cycling a material between a field of –H and H. Eddy current losses are losses at high frequencies related to the material's electrical resistivity. Saturation induction, B_s, is important to provide a large induction in a small size device. Curie temperature is the temperature at which magnetic ordering in the material is lost. Some material properties for common soft magnetic materials [56] are given in Table 1 below.

Table 1: Properties of Some Common Soft Magnetic Materials[56]

	Permeability	Saturation Induction	Curie temperature
Bulk Materials			
Silicon steel	10^4	1.6-1.8 T	750°C
Supermalloy	10^6	0.6-0.8 T	400°C
Hiperco	10^3	2.0-2.45 T	930°C
Ferrites			
Mn-Zn	10^4	0.3-0.5 T	100°C-250°C
Ni-Zn	10^3	0.1-0.36 T	100°C-500°C

Bulk ferromagnetic materials for power transformers are typically silicon steels that are processed into thin sheets and laminated. These are limited to low frequency (60 Hz) and

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moderate frequency applications. Amorphous metal magnets can possess much higher permeabilities and resistivities, which provides advantages in frequency response. However, synthesis of these alloys requires stabilization of the glassy phase through the addition of a significant fraction of non-magnetic glass forming species. This reduces the saturation induction and Curie temperatures of these materials. Furthermore, the alloys have relatively low crystallization temperatures. This makes them unstable for use at elevated temperatures, especially above 300°C. High resistivity ferrites are also limited in their operation at elevated temperatures, as many interesting high frequency ferrite materials have Curie temperatures below 300°C. A promising new option for high temperature power applications are nanocrystalline and bulk amorphous magnetic materials [57]. Such materials have been shown to have excellent properties at high frequencies (10-100 kHz range and higher). These materials possess saturation induction values of 1.6 – 2.1 T, which are three to five times those of ferrites and twice those of amorphous magnets, allowing for proportional reduction in component size. Furthermore, nanocrystalline soft magnetic alloys have been developed over the past decade with high permeabilities, high Curie temperatures, and without the magnetic hardening associated with the crystallization of amorphous alloys. This limits the core losses. Core losses can reduce efficiency and increase the temperature of surrounding components leading to failure well below the Curie temperature [58]. Fe-based nanocrystalline alloys, such as FINEMET and NANOPERM, however, suffer problems at elevated temperatures associated with the decoupling of the exchange interactions between nanocrystals. A new Fe-Co based nanocrystalline alloy, HITPERM has been shown to retain excellent magnetic exchange coupling and other properties at temperatures as high as 500°C – 600°C, making it an excellent candidate for use in high temperature electronic applications [59-61].

Resistors have been shown not to be a major concern, as most thick film surface mount chip resistors and thick film paste resistors, such as the Heraeus-Cermalloy 900 Series, perform reliably after many hours at 300°C and above [62]. These resistors are made of a fired RuO_2 paste on an Al_2O_3 insulating ceramic base with a silver inner electrode and a nickel outer electrode. They have good temperature stability in the range 300°C to 500°C with a thermal coefficient of resistance of ± 200 ppm, owing to their manufacture at temperatures of 500°C-1000°C. They exhibit a resistance drift of only a few percent after 2000 hours at 300°C – 400°C. The ultimate limit to their use is softening of the glass frit at temperatures above 500°C [62]. Thin film surface mount chip resistors consist of a vacuum deposited film of TaN or Ni-Cr on an Al_2O_3 base. High temperature versions, using the Ni-Cr film, are less thermally stable than thick film resistors, and have a maximum operating temperature of 200°C to 300°C [62].

Wirewound discrete resistors, such as the power resistors made by Dale, are made of a resistive wire (NiCr, CuMn, FeCr) wound around a ceramic bobbin with Au plated Ni axial leads and end caps. These high precision resistors are stable under powered/unpowered aging to 300°C and some commercial version are capable of 500°C operation. This is not true of film or carbon composition resistors, which are not recommended for use at elevated temperatures [62].

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PC Boards

Traditionally, the push to use ceramic substrates for high temperature electronics has resulted from concerns related to the use of standard FR4 organic board material at temperatures above 135°C, its glass transition temperature (T_g). Printed wiring boards (PWB) and substrates must provide mechanical support for components, thermal dissipation, and electrical interconnection. Above T_g, organic boards begin to lose mechanical strength due to resin softening, and exhibit large discontinuous changes in their out-of-plane coefficient of thermal expansion, which can cause in-board delaminations and loss of adhesion to the copper traces. In addition, organic boards exhibit significant decreases in their insulation resistance above T_g.

Advances in materials technology, however, have produced a number of organic laminates with T_g in excess of 135°C, including bismaleimide triazine (**BT**), and high temperature, tetrafunctional FR4 materials, which operate to 180°C. Boards based on cyanate ester or polyimides can be used at temperatures as high as 260°C. The glass transition temperatures and key electrical and mechanical properties of many of these new materials are provided in Table 2 shown below:

Table 2 Properties of organic printed wiring board materials [63, 64]

Material	Supplier	Tg (°C)	Dielectric Constant	CTE-Z ppm°C	CTE-X ppm°C	CTE-Y ppm°C	Approximate Cost Adder over Fr4	Dissipation Factor @ 1 MHz
FR4 Tetrafunctional	Polyclad Nelco N4000-2	135 142	4.5	60	15	15	Tetrafonctional 1 (baseline)	.019
FR4 Tetra II #370	Polyclad Nelco N4000-6	175	4.4	60	15	15	1.2x	.012
FR4 Tetra II Plus #370-G	Polyclad	180	3.9	45	14	14	1.3x	.010
Getek	G.E	180	3.9	50	13	13	1.4x	.013
B-T	Norplex/Oak Nelco N5000	180	4.1	50	13	13	1.5x	.015
Thermount	Nelco N7000-2T	220	4.1	85	8.5	8.5	3.5x	.022
Polyimide Blend	Nelco N7000-2	225	4.3	70	13	13	2.5x	.014
Cyanate Ester E-Glass	Nelco N8000	250	3.8	55	12	12	2x	.009
Cyanate Ester S-Glass	Nelco N8000S	250	3.6	50	9	9	6x	.009
Polyimide 85NT	Arlon	250	3.9	100	6-9	6-9		.015
Polyimide E-Glass	Nelco N7000-1	260	4.3	70	13	13	3x	.013

E-glass/ PTFE laminates have a T_g greater than 300°C, but are not recommended for use above 120°C because of weakening adhesion of the copper layer, although advances in this technology are continuing.[63, 64]

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Problems with these polymer based board materials [65] include the following:

1) The resins that have high glass transition temperatures, such as CE, PI, and BT, also have high cost.
2) While PTFE is used for digital and microwave applications requiring low dielectric constant and dissipation factor, Cu-clad PTFE is thick and heavy, with poor thermal dimensional stability, and a CTE as high as Cu in plane and even higher out-of-plane.
3) The CTE mismatch between silicon and the board material cannot be tolerated by flip chip interconnections.
4) Use of underfills and silicone elastomers to mitigate CTE mismatch is not possible for high temperature applications as these materials are not fit for high temperature use and cannot withstand large numbers of wide temperature cycles. Three underfill materials have been identified for use to 150°C. These materials have more crosslinking leading to a higher glass transition temperature, higher CTE, lower modulus, and better adhesion. However, none have been proposed for 175°C. [66]

A new polymer-based film, PIBO, has been proposed to address these issues. PIBO is a high temperature stable polyimide film with resistance to plasma degradation. The film has high strength and stiffness, low dielectric constant and dissipation factor, and excellent thermal properties. It has a CTE of 3 ppm/K and it does not exhibit a glass transition temperature, Tg, or a melting point, Tm, up to 600°C. Direct bonding of copper as opposed to adhesive bonding is possible using plasma followed by sputtering and subsequent electroplating. This film has demonstrated a life of more than 2000 thermal cycles making this material promising for automotive applications that require shock and vibration combined with temperature cycling. [65]

The critical failure mechanisms which limit the use of PC boards at high temperatures are delamination of the copper from the laminate and delamination within the laminate, conductive filament formation, and PTH fatigue and separation. These are discussed in further detail below.

Delamination

Delamination is defined as a separation between the layers of the printed circuit board (PCB), such as between the FR4 and the copper foil, or between the epoxy resin and the glass fiber.[67] The latter form of separation can lead to a reduction in insulation properties by entrapping processing solutions and can provide a path for conductive filament formation. Delamination is a particular issue in high temperature applications, both because of the use temperatures and also because of the temperatures needed for assembly with high temperature solder materials, where the reflow temperature is well above that for standard tin-lead solder.

Delamination occurs when environmental stresses resulting from temperature changes, mechanical bending, and/or moisture, exceed the interfacial strength. Delamination is especially prevalent when the Tg of the polymer resin is exceeded, because of its large,

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discontinuous increase in CTE above Tg. This results in a high CTE mismatch between the resin and the glass or between the resin and the copper. Delamination stresses are thus increased over those for the same change in temperature in a material that is still below its Tg. This makes the use of high Tg materials like polyimide preferable for high temperature applications. The maximum acceptable temperature for polyimide is about 260°C, while that for G-10 and FR-4 is only about 135°C. The electrical characteristics of polyimide are similar to epoxy, but polyimide has improved chemical resistance. The disadvantages of polyimide are its high price, poor peel strength (half of copper-clad epoxy at room temperature), higher cure temperature (220°C versus 175°C for epoxy), and longer post-cure time.

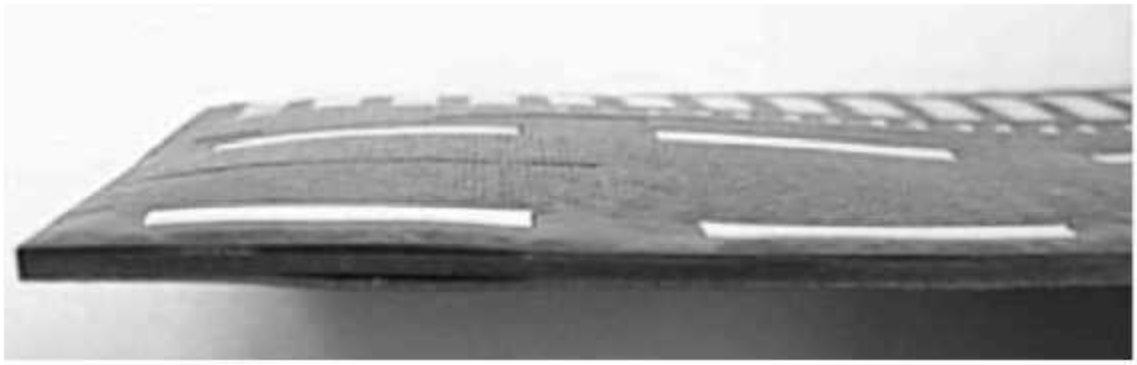

Figure 8 Delamination of copper above Tg, Cyanate Ester at 250°C.

An additional factor that should be considered for printed circuit boards for automotive use is the fact that at higher temperatures the absolute volume expansion and contraction of the epoxy-resin outside the bundles is much greater than that inside the bundles, increasing the thermal stresses during thermal cycling at the glass-fiber bundle edges. Once the stresses exceed the bonding stress, delamination can occur. In terms of resistance to severe thermal excursion, cyanate ester boards provide greater performance than the widely used FR-4 [68].

Conductive Filament Formation

CFF is an electrochemical process that involves the transport (usually ionically) of a metal through or across a non-metallic medium under the influence of an applied electric field [69-71]. CFF is a potential reliability problem, in that it can cause current leakage, dielectric breakdown and electrical shorts between conductors. The biased conductors act as electrodes providing a driving potential while ingressed moisture between the organic resin and the fiber reinforcement will serve as an electrolyte (see Figure 9). As metallic ions migrate and form a bridge between two biased conductors, the loss of insulation resistance results in a current surge. The current surge will eventually result in a short and a large increase in localized temperature. This increase in localized temperature can manifest itself as a burnt or charred area between the two conductors.

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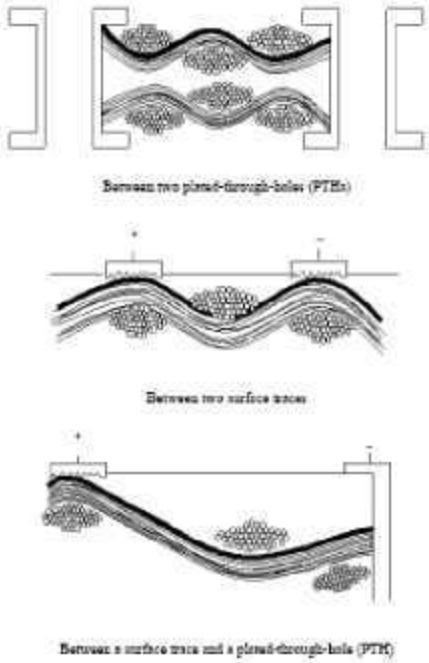

Figure 9 Conductive filament formation (CFF) configurations[72].

The prime factors influencing CFF are board features (resin materials, conformal coatings, and conductor architecture) and operating conditions (voltage, temperature, and relative humidity). The accelerating effects of temperature and relative humidity make this mechanism of specific concern in automotive applications. Furthermore, path formation, necessary for the occurrence of CFF, will occur due to interfacial delamination of the interface between the individual fibers and the organic resin matrix. This degradation is often due to thermal cycling (see Figure 10) and is exacerbated by use of the board over its Tg as discussed in the previous section on delamination. Previous studies have gathered data on the quantitative effect of these various elements [73-75].

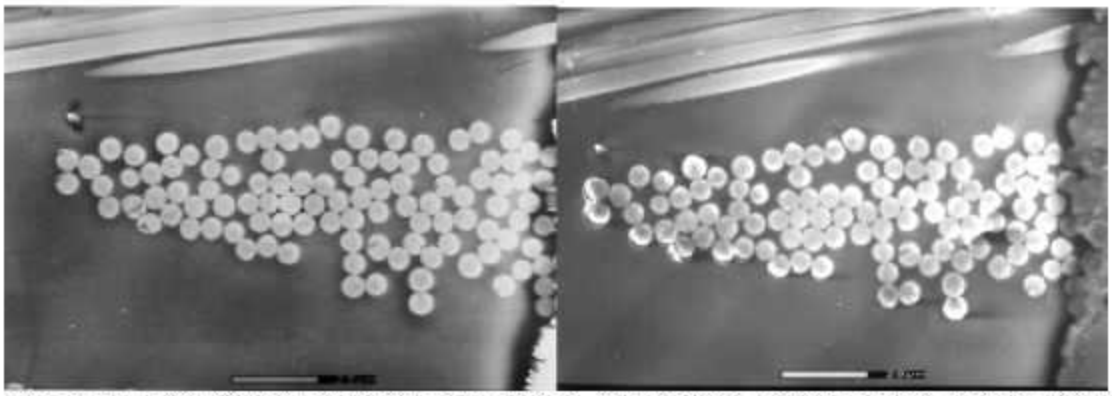

Figure 10: Left: (820x) Before thermal cycling, this electron micrograph of a fiber-reinforced laminate shows good interfacial bonding at the fiber/epoxy resin interface prior to thermal cycling. Right: (820x) After thermal cycling, several instances of interfacial degradation (debonding) can be seen to have occurred at the fiber/epoxy resin interface[72].

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Based upon this empirical evidence, models have been presented that predict the operational lifetime assuming an eventual failure mechanism of CFF [75, 76].

Experiments have shown that CFF can also occur in the presence of hollow fibers [77, 78]. The environmental considerations are the same, however in this case the path formation occurs within the fiber itself, instead of along the fiber/matrix interface. The scenario of electromigration within the fiber and its effect on time-to-failure has also been modeled [79].

Plated Through Hole (PTH) issues

Plated through hole (PTH) misregistration can lead to cracking between adjacent PTH's. This crack can serve as a path for CFF (Figure 11). The time for CFF is also accelerated because the distance between two PTH's or a PTH and a transmission line is shortened through misregistration.

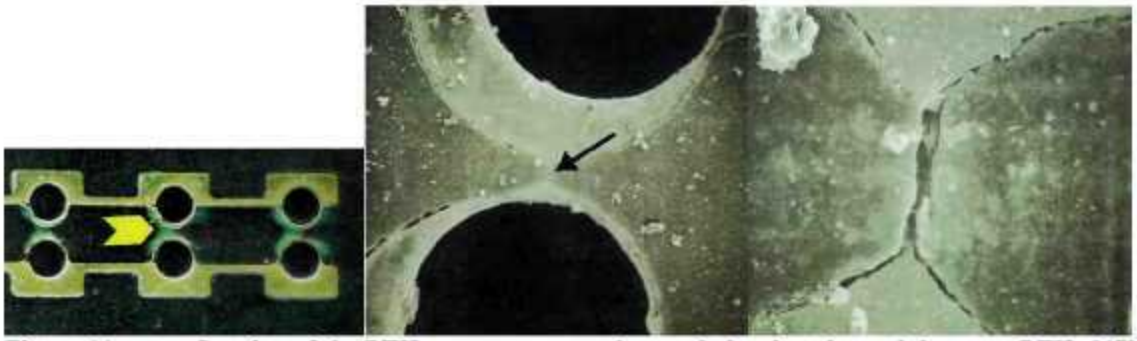

Figure 11 Spacing of the PTHs not propper and a crack developed a path between PTHs [67].

Besides being a contributing factor to the development of conductive filament formation through hole technology presents a number of other elevated temperature use concerns over surface mount technology.

PTHs are normally created by a drilling process. Any burrs or resin smear covering inner layer interconnects are removed. Deburring slightly roughens the hole and allows for subsequent plating. The hole is then coated by electroless copper deposition. The thickness of the electroless layer is typically 80 to 100 millionths of an inch. The barrel of the hole is then electroplated with copper to a thickness of one mil.[80]

For automotive environments, PTHs may see the following failure mechanisms:

- Fatigue Crack in PTH Wall
- PTH Wall Pad Separation

A fatigue crack in the PTH Wall is a crack that propagates around the circumference of the PTH or Via due to cyclic stresses that exceed the fatigue strength of the copper wall [67]. PTH fatigue cracks usually occur in the field and can be a cause of infant mortality. They are generally a result of poor design, a non-optimized manufacturing process, defective material or customer misuse. Poor design can be difficult to discern and may require stress analysis or accelerated testing (such as interconnect stress testing (IST)),

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especially if the product is leading-edge technology. Besides fatigue fracture occuring from CTE mismatch between the PC board and the PTH, this failure can also occur at elevated temperatures due to PTH wall recession. The PTH wall recession is when resin has backed away from the hole wall. As the temperature rises, the material becomes more flexible and this failure becomes more likely. Above Tg, the resin material becomes very soft.

PTH Wall-Pad Separation is separation of the inner layer pads/lands from the PTH due to stresses that exceed the adhesion strength. A picture of wall separation, also known as breakout of internal lands, can be seen in Figure 12

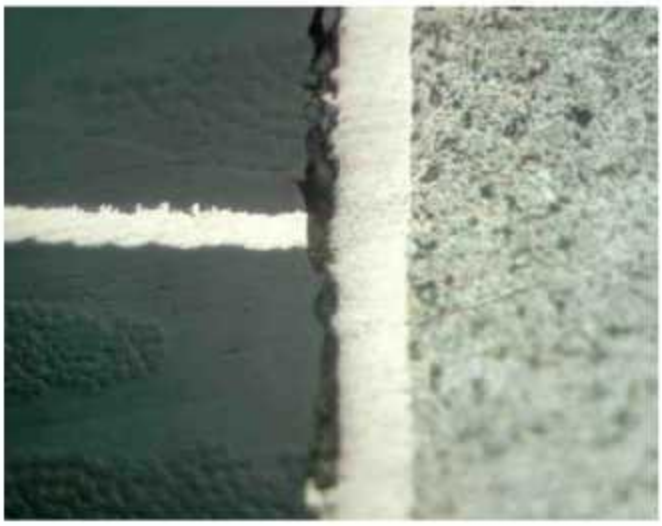

Figure 12 Example of PTH wall separation [67].

PTH Wall separation usually occurs during printed board manufacturing and assembly, which indicates an overstress mechanism. Separation can also occur during the field, but this is often an indication of a separation that occurred during manufacturing or assembly that was not detected, or did not fully propagate, until operation. The wide temperature ranges seen in automotive applications can serve to propagate the separation, especially if the Tg is exceeded. Note that wall separation is not resin pullback.

Surface mount versus through hole technology

Assembly processes are classified based on attachment configuration as follows: through-hole assembly, surface-mount assembly, and mixed through-hole and surface-mount assembly. Through-hole assembly involves inserting component leads into plated through-holes (PTH) in the board and soldering them. [81]. In surface-mount assembly, the component leads are soldered to the surface of the printed wiring board. The solder joint, now the sole mechanical and electrical connection between the printed wiring board and the component, bears a significant amount of the stress from any vibrational or thermomechanical loads on the board. [81].

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The main difference between these two technologies for use at elevated temperatures is in the dominant failure mechanism. In the surface mount technology, the main concern is the delamination of the copper pads and layers from the resin, while in the through-hole technology it is the fracture of the PTHs. In addition, high temperature operation is more of a concern for surface mount assemblies than for through-hole assemblies, because of the greater strains on the solder joints in surface mount technology which makes SMT assembly reliability more sensitive to wide temperature swings than through-hole assembly reliability.

Limitations in number of layers

PC boards can be manufactured in single sided, double sided, or multilayer form factors, which can contain up to 24 different layers. Typically the need for a multilayer board comes from complex signal routing in computing or RF applications. Typical PC boards used in power applications have 2 to 4 layers, where 2 are used for signal currents and 2 are used for power currents. Since the currents carried by the copper layers in the board are significant, self heating of the conductor layers is an issue and is typically addressed by adding more area to the board or using thicker copper layers.

There is no established rule of thumb for the number of layers allowed at any temperature. However, it stands to reason that strain in the resin and between the resin and the copper layers due to CTE mismatch and the subsequent susceptibility to delamination will increase slightly with increasing numbers of thicker copper layers. Therefore, at higher temperatures, especially above Tg, and wider temperature swings, it is may be necessary to use a smaller number of thinner copper layers to minimize strain. This may require a trade-off, however, in power boards where the increased temperature makes it more important to have thicker copper layers to limit the power dissipation and subsequent additional heating. In addition, it may be necessary to limit the overall thickness of the board, as well, to minimize the axial strains on PTHs and vias, caused by CTE mismatch that can result in PTH or via plating fracture.

Packaging types

The power electronics that are used in the inverters of a hybrid electric vehicle consist of power switching devices, diodes, capacitors, resistors, and inductors, all of which have been discussed above. However, there is another critical factor in reliable operation of these electronic systems at elevated temperatures and that is the associated packaging.

Typical inverter modules are three-phase pulse width modulated (PWM) devices each with six arms. Each arm consists of one power switch and its associated free-wheeling diode. The typical power switch is an insulated gate bipolar transistor (IGBT), although power MOSFETs or thyristors can be used instead. The power switches and diodes are attached to direct-bonded copper (DBC) aluminum oxide (or nitride) substrates using a

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lead-based or lead-free solder. The substrates are, in turn, attached to a copper heat spreader using the same metallic solder. The IGBTs and diodes are then interconnected by one of several different technologies. [82] The most common of these different technologies for packaging and interconnection of the devices are provided below.

Chip and Wire Package

Chip and wire packages use multiple thick wires to interconnect the top surfaces of the die to each other, to the DBC substrate, and/or to I/O pins on the side of the module. For current chip and wire technology, gold or aluminum wires are used as interconnections. An example of a wire-bonded module can be seen below. These modules are widely available from all major power electronic device manufacturers including Semikron, ABB, Toshiba, Siemens, and others.

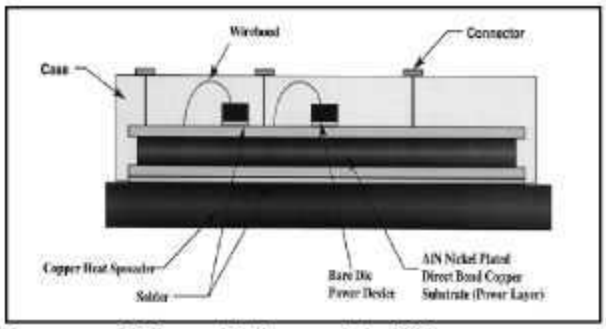

Figure 13 Chip and Wire module.[83]

While this process utilizes well-known technology and a simple, low-cost fabrication process, it has several disadvantages. First, it is prone to noise, oscillations, and fatigue caused by large currents passing through the wires. Also, large electromagnetic fields are generated as currents pass through adjacent wires, thus creating uneven current distributions among the wires. Another disadvantage of wire-bonds is that all cooling must occur through the bottom of the die, which greatly restricts heat dissipation from the module [84]. This, combined with the localization of current flowing into the top of the device, creates hot spots on the top surface of the die at each wirebond. These hot spots are also areas of high temporal thermal gradients when power is rapidly switched on and off. Lastly, wire-bonded modules have a low power density and a low silicon-to-footprint ratio due to their packaging structure[85].

Several reliability studies of wire-bonded power modules have shown that the wire-bond is the dominant failure site. This is due both to wire flexure fatigue resulting from the wide ambient temperature swings in automotive environments and to wire liftoff resulting from the creation of these hot spots and high thermal gradients at the wirebond-to-die interface at the top of the device. Additionally, the large solder area of the bond can fatigue and delaminate under thermal cycling [84] resulting in poor heat transfer over large areas of the attach under the die. This increases the temperature of the hot spots above these areas, accelerating wire liftoff failure. These two packaging technologies, wirebonding and die attach, critical to reliable operation of chip and wire modules are

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discussed in detail below. Despite these reliability weaknesses, wire-bonds are still the most common interconnection technique in today's microelectronics packaging.

Wirebond

Wires and wirebonds are subject to failures in high temperature electronic systems as a result of the wide temperature excursions. The thermal expansion mismatch between the chip and the substrate in unencapsulated cavity packages, and between the chip, the substrate and the encapsulant in silicone filled power modules or in small signal plastic encapsulated microcircuits, generates a significant thermo-mechanical stress in the internal interconnection wires joining these elements, particularly when thermal cycles from -55°C to 200°C are encountered. The failures seen from thermo-mechanical stresses are wire flexure fatigue caused by the thermal mismatch between the wire and the substrate in encapsulated and unencapsulated modules, along with shear of the bond pad (wire liftoff) due to the thermal mismatch between the bond pad and the underlying substrate, and finally failure due to axial tension of the wire caused by the thermal mismatch between the wire and the encapsulant in which it is enclosed.[86] The highest concentration of expansion stresses is at the wire terminations, where the wire is immobile and unable to flex to accommodate the strain. Typical failure sites for flexural fatigue are the neck of a ball bond, and the heel of a wedge or stitch bond. The failure site for wire lift-off is the bond interface between the wire and the bond pad; and the failure site for axial fatigue is in the middle of the wire length. The location of the failure is dependent on the relative strength of the wire and the wirebond, and new models for this failure mechanism are being developed [87].

Further research in the area of fatigue of aluminum wirebonds would be very advantageous for improving power electronic module reliability. As power devices switch to copper metallization, research into copper wire-copper bondpad liftoff is also needed.

High temperature applications can also weaken both the wire and the wirebond by annealing of the wire and intermetallic reaction at the bond site, respectively. Annealing is the removal of damage and defects induced in the wire during the low temperature portion of the thermal cycle by recrystallization and grain growth during the high temperature portion of the thermal cycle. The larger grains reduce the strength and fatigue resistance of the wire. This effect is particularly pronounced in the neck of gold ball bonds. The second effect, intermetallic reaction, takes place in the following manner. Two dissimilar metals placed in contact diffuse into each other at different rates, leaving behind a supersaturation of vacancies on the side of the fast diffusing metal. These vacancies coalesce into voids, known as Kirkendahl voids, which act as stress concentrators, reducing the fatigue resistance of the wirebond. The two metals may also react with one another forming one or more intermetallic phases. These phases typically have complex crystal structures, and thus are usually brittle and more susceptible to

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fatigue flexure damage than the pure metals. When the component is then exposed to differential thermal expansion stresses, fracture often initiates at the voids and propagates through brittle intermetallic layers, causing failure at the bond site [88].

Wirebond degradation resulting from intermetallic reaction is often seen in the Au wire and Al bond pad wirebonding system typically used in commercial integrated circuits. The intermetallic formation process is governed by the diffusion of gold into aluminum, with Au_5Al_2 forming first followed by $AuAl_2$. The higher diffusivity of gold leads to voiding on the gold side of the interface. Below 175°C, intermetallic growth in the gold-aluminum system is not primarily dependent on steady-state temperature, but rather on the defect density [89], with poorly welded joints failing by interdiffusion and intermetallic formation at times and temperatures significantly less than those predicted from lattice diffusion alone. In fact, intermetallics have been observed to form at temperatures as low as 75°C in joints having many grain boundaries, vacancies, and dislocations. However, in well bonded systems, an intermetallic-related decrease in bond strength is not observed in use at temperatures less than 125°C [90, 91]. Intermetallics are not a concern in chip and wire power modules as the bonding on the die is almost exclusively mono-metallic (i.e. Al wires to Al bond pads). There can be a concern between the Al wires and the Au plating on the DBC or the copper on the DBC. However, the use of nickel plated DBC will eliminate this concern, as Al wires on Ni plated DBC have not been seen to exhibit intermetallic formation at 1000 hours at temperatures up to 350°C [92].

Chip and Substrate Attachment

Chip and substrate attachment refers to the use of conductive and non-conductive adhesives to attach the silicon chip to the underlying substrate, and the use of similar adhesives to attach the substrate to the underlying heat spreader. Die attach in power modules has three main functions. First and foremost, it has the mechanical function of holding the chip in place and affixing it to the substrate. Next, it has the thermal function of providing sufficient heat transfer from the chip to the package to permit the device to operate at high power without exceeding its maximum operating temperature. Finally, it has the electrical function of providing an electrical contact between the chip backside and the wiring on the substrate. This electrical function is specific to power devices and is a result of the fact that the backside of the die is typically electrically active. This is different from planar small signal devices where all the interconnections are made from the top surface of the die. As a result of this electrical function, die attaches for power devices must be highly electrically conductive. As such, power die attaches are typically made of metal alloys as opposed to the filled polymers which are typically used to attach small signal devices.

The most critical reliability concern for die attach is fatigue cracking and delamination leading to die debonding. Die debonding is the dominant failure mechanism for chip and wire modules subjected to passive thermal cycling, such as would be the case for changes in the ambient temperature under the hood of an automobile. While eventually, die debonding will progress to the point where the die becomes detached from the substrate,

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failure of the device will most likely occur much earlier. Failure typically results from the increase in thermal impedance that comes in the initial stages of die debonding. Low thermal impedance is critical to keeping chip temperatures in the range of reliable operation. Die debonding reduces the heat transfer, leading to overheating of the die which results in both parametric and functional device failure. Die debonding can be caused either by fatigue crack growth in the bulk die attach, or by deadhesion of the solder at the interface. Deadhesion is due to manufacturing defects such as poor wetting of the solder to the interface metallurgy, voiding in the solder, or the presence of dross in the solder. As such, it is to be controlled through the proper choice of soldering materials and proper manufacturing parameters.

Fatigue cracking, on the other hand, will occur whenever the solder is subjected to a thermo-mechanical stress/strain field resulting from expansion mismatch between the die and the underlying substrate during temperature cycling. The most obvious source of these stresses and strains is the global coefficient of thermal expansion mismatch between the components and the substrate in addition to a more local CTE mismatch between the component and solder, and the solder and substrate.

The high power requirements of power devices combined with the need for high electrical and thermal conductivity has led to the widespread use of tin-lead based solders as die attach materials. Examples of typical die attaches are Pb10Sn, Pb5Sn, Pb5Sn2.5Ag, Pb2Sn2.5Ag, and Sn37Pb. These solders are often grouped by melting point, with the low melting point solders being preferred for applications where the operating temperatures are relatively low and the chips are large (less than 1 cm x 1 cm) as would be the case for silicon power devices, while the high melting point solders are preferred for applications where the operating temperatures are high and the chips are small (less than 1 cm x 1 cm) as would be the case for SiC devices. In addition to these lead-based solders, one lead-free solder has been widely used, Sn25Ag10Sb, also known as J-alloy. This lead-free die attach, while used in some plastic packaged components, has a number of drawbacks, including a high price and poor manufacturability. Other lead-free solders, such as Sn3.5Ag, have been used in moderate temperature applications, $-20°C < T_{amb} < 100°C$, but have some reliability concerns related to the size and distribution of Ag_3Sn intermetallic particles. These intermetallics can strengthen the die attach when they are small and well distributed, but act as crack initiation sites when large and concentrated. The natural tendency is for the intermetallics to coarsen with time at temperature. This tendency toward intermetallic coarsening, combined with a relatively low melting point of 217°C and poor reliability under thermal cycling at Tmax > 125°C, makes this solder ill-suited for high temperature applications. This is also true for many of the ternary and quaternary versions of this solder, which add small amounts of Cu, Ni, Sb, and Bi to improve reliability.[93],[94] Sn-0.7Cu is another copper containing tin-based solder that exhibits a similar microstructure and similar properties to Sn-3.5Ag. However, in addition to high temperature fatigue concerns, the high tin content makes this solder prone to whisker growth.

Gold-based eutectic alloys (i.e. Au12Ge, Au3Si, and Au20Sn) are an option for high temperature soldering, because of their excellent creep and corrosion resistance together

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with high strength. However, these alloys are very expensive and hard to process. In addition, their hardness and brittleness causes them to transmit rather than absorb a great deal of the thermomechanical stress of the joint [95].

Another approach which is now commercially available in a number of inverter modules, including ones from Semikron, is attachment by means of high temperature sintering of noble metal powders. This technology provides the ability to create attachments at low temperatures (< 300°C) that are reliable to very high temperatures (>900°C). In particular, silver powder is preferred because of its high electrical and thermal conductivity, its high melting point (960°C), its high fatigue resistance, and its low cost relative to gold.

The approach most widely used at present is based on the work of Schwartzbauer [96] who originally proposed the low temperature sintering of small (sub-micron) silver flakes that are dispensed as a paste onto the substrate surface. With this approach, joints are made at 220°C – 250°C, a temperature well below the melting point of silver, at pressures of about 40 MPa in one minute in air [96]. It is believed that applying external pressure assists the densification process by eliminating some fraction of pores through compression/deformation, thus increasing the contact area between the silver particles [97]. In this strategy, a hot press is used to apply a quasi-hydrostatic external pressure on the device assembly. Commercial silver paste with a particle size in the range of 1-3 μm can also be used [97]. The finished joint typically has a porosity of 80-85%, a thermal conductivity of about 250 W/mK, and electrical conductivity of 40 MS/m. The thermal and electrical conductivity are consistent with pure silver of similar porosity [98], and are significantly better than those of eutectic SnPb die attach. The adhesion strength of the sintered silver joint was also found to be higher than that of the eutectically soldered joint [97]. Furthermore, the uniform microporous silver microstructure provided additional compliance which acted to relieve the thermo-mechanical stresses due to CTE mismatch, thus improving the joint reliability under thermal or power cycling. Joints made in this way have shown a twenty times improvement in power cycling reliability at $\Delta T_j = 130°C$ over that of eutectic solder joints in standard modules, as determined from an extrapolation of the reliablilty model [98].

The application of external pressure has a drawback because it makes automation in manufacturing very difficult to implement and thus increases the cost [99]. Furthermore, applying pressure may cause device cracking [99]. Alternative methods are therefore being researched to lower the needed pressure by using either Ag and Au nanopowders [100]. The reduction in the size of the powders to the nanoscale increases the surface energy of the particles, which then increases the driving force for agglomeration, reducing the pressure needed for the sintering operation [101]. Nevertheless, it appears that a pressure of around 4 MPa and a temperature of 250°C-300°C is still necessary for bonding. Furthermore, the high levels of liquid binder needed in the colloidal suspensions used to deliver the powder are difficult to bake out from under large die, resulting in high levels of voiding. In addition, these high binder levels result in microcracking of the attach due to shrinkage upon drying and firing. Other limitations of

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this technique include the fact that silver powder bonds poorly to nickel or copper. This means that DBC substrates must be silver or gold plated for good adhesion. However, the silver or gold plating will create intermetallic formation problems with Al wires bonded to the substrate. Therefore, selective plating of the substrate is required – a costly and difficult process. Another concern with this technology is the tendency for silver to migrate under bias, and the high cost and stiffness of gold attach.

Use of solder in the liquid state has also been proposed. In particular, the Nb-In-Sn system has been considered for the development of liquid solder joints at 192°C. However, it may take up to one month to get sufficient intermetallic to form a good solder joint. Also the reliability of containing a liquid solder interconnection is questionable at best.[102] Similarly, liquid phase transient bonding has been proposed, but the length of time needed for sufficient solid-state diffusion to occur to form a bond is often greater than desired from a manufacturing standpoint [103]. Nevertheless, this approach does hold promise.

Further research on the reliability of sintered silver nanopowders and other high temperature solder techniques is needed.

Substrate

Ceramics are the traditional substrates for use above 125°C. There are three ceramic materials which have traditionally been used for substrates in this approach, the properties of which are given in Table 3 shown below:

Table 3 Properties of ceramic substrate materials[104]

Material	Thermal Conductivity (W/mK)	Thermal Expansion (ppm/K)	Dielectric Constant @1MHz	Loss Tangent @ 1 MHz
AlN	170	4.6	8.6	0.0005
Al_2O_3 (96%)	25	7.4	9.0	0.0001
BeO	260	8	6.5	<0.0004

Aluminum oxide (Al_2O_3) is the preferred selection for low cost applications. The disadvantage of Al_2O_3 is its poor thermal conductivity, which makes it acceptable for systems which operate in high ambient temperatures, but not acceptable for systems where a significant fraction of the heat is generated by the die and must be dissipated through the substrate, such as power conditioning systems. For high temperature, high value, power electronics, AlN is the preferred choice [104-107] because of its close thermal expansion match to both Si and SiC, and its high thermal conductivity, as shown in Figure 14 and Figure 15. In recent years, the improved metallization and lower cost of AlN has driven BeO, with its toxicity concerns, from the market.

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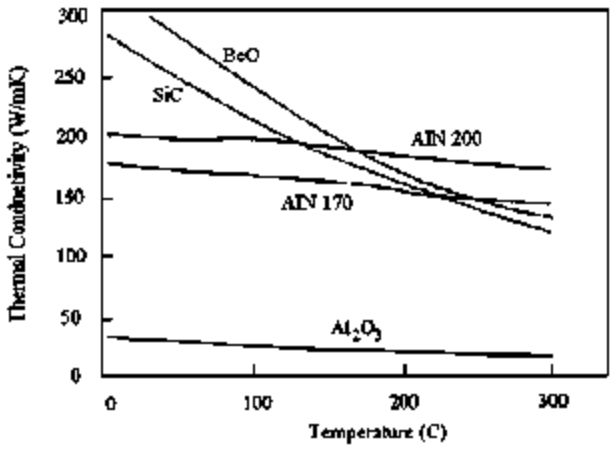

Figure 14 *Thermal conductivity of ceramic substrate materials [107]*

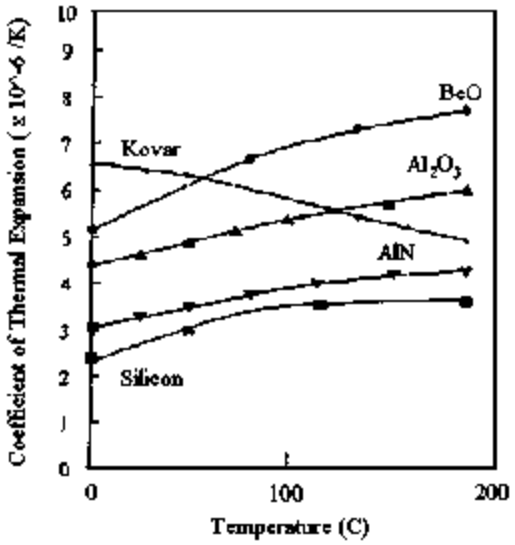

Figure 15 *Thermal coefficients of expansion (CTE) of ceramic substrate materials [105]*

These substrate ceramics can be processed in a number of different ways. Low Temperature Cofiring (LTCC) is useful for small signal substrates that have a maximum use temperature of 300°C. Above this temperature, the noble metals used for metallization begin to degrade and delaminate and it is necessary to switch to High Temperature Cofiring, which uses more thermally stable, but lower conductivity, refractory metals. High Temperature Cofired Ceramics (HTCC) can be used up to 500°C.

Power substrates are typically manufactured using direct bonded copper (DBC) techniques. Direct bonding of copper is done by creating a ceramic eutectic joint between copper oxide and aluminum oxide at the copper interface to either aluminum

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oxide or oxidized aluminum nitride. This approach is used in order to bond a layer of copper on the ceramic that is thick enough to handle the large currents in power applications. The bond is extremely strong and will not delaminate. The failure mechanism in wide temperature range cycling is brittle fracture of the ceramic under the copper due to localized CTE mismatch.

In addition to being considered as a possible high temperature power semiconductor material, SiC is also being investigated as a possible high temperature insulating board or substrate material. This is because co-fired ceramic boards are expensive, have poor thermal conductivity, and are easily cracked under shock loading. All these problems can be solved, if metal traces and alternating layers of ceramic are bonded to silicon carbide without co-firing or the use of glues. SiC is a good heat conductor, is very strong, and can be used in layers along with conductive vias. In work at the Idaho National Engineering and Environmental Laboratory, conductive traces were mechanically bonded by plasma spray or electroplating onto SiC with sufficient bond strength to remain functional at 350°C. There was no deterioration of current capability in these traces with temperature cycling. These traces can be used to propagate signal or power, act as temperature indicators, or act as component attach. Three passes of the spray gun leave a Ni – 5% Al trace that is 1.5 mils thick over a 0.8 mil thick plasma sprayed alumina insulating layer.[108]

Another substrate that is being explored for power modules is silicon nitride, Si_3N_4. Its advantage is a fracture toughness which at 5 MPa-$m^{1/2}$ is twice as high as Al_2O_3 or AlN. This leads to the ability to survive more and wider temperature cycles. However, silicon nitride cannot be metallized using DBC techniques and must have the metal applied using active metal brazing. This results in an inferior adhesion that causes early failure due to delamination. In addition, silicon nitride substrates are currently in very short supply.

Further research into silicon nitride substrates and their metallization is in order.

Double Sided Attach Module

The double sided attach approach is a three-dimensional packaging technique that provides high electrical and thermal conductivity. In this approach, each semiconductor device is sandwiched between a metallized ceramic lid above the die and a metallized ceramic substrate below the die. The device is attached to the lid and substrate by reflowed solder or other similar attach material. A simple manufacturing process is followed, making only three connections (source, gate, and drain)[109].

The ThinPak™ is an example of a double-sided attach module. In this package, the lid is soldered directly to the top surface of the chip with a high lead (Pb10Sn) solder. A pattern of metallized holes in the lid permits the solder to flow through, providing electrical conductivity through the lid. The top side of the lid is bonded with eutectic solder (Sn37Pb) to a copper strap that forms the anode terminal. In later versions, the copper straps are eliminated and connection to the source and gate is made integral to the

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lid, which is now a piece of DBC alumina, and connection to the drain is made integral to the DBC substrate. An optical micrograph image of a direct solder package is shown below. Power modules using this technology are available from SPCO, while encapsulated single chip packages using this technology are available from International Rectifier, Vishay, and others.

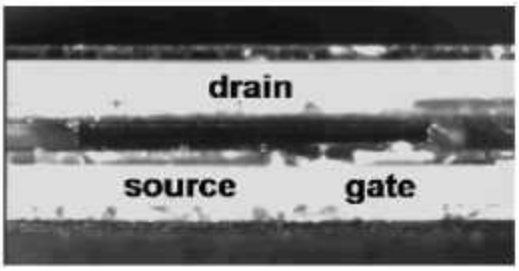

Figure 16 **Direct solder interconnect [109]**

The main advantage of this approach is the ability to cool the device from both sides, leading to improved heat transfer for high power dissipating components. A double sided attach module can dissipate up to 50% of its heat through the lid. Also, the very large contact area, provided by the copper leads, permits larger currents and lower thermal resistance, which improves the thermal management of the package. Other advantages include the elimination of wire bonds in this package, which results in the absence of wire bond related failures. Furthermore, the removal of wirebonds reduces package inductance (~0.5 nH), thus increasing switching speed and current rating. In addition, the inherent low forward voltage drop in ThinPak^{TM} (<1.5V at > 100A/cm^2) [110] when combined with the low electrical resistance of the lid greatly reduces power dissipation levels up to switching frequencies of several tens of kHz. Thus, this technology offers one of the highest areal (>90%) and volumetrically efficient approaches for packaging discrete power semiconductor devices, while improving heat transfer.

There is a drawback, however, to the large contact area of the straps or DBC lid/substrate, in that it leads to stresses caused by large CTE mismatch. Cracking in the solder attach at the die-to-DBC interface can be a failure mechanism in these modules due to the CTE mismatch between the DBC ceramic and the die. In modules where the final connection is made by soldering copper straps to the DBC, instead of by integral connections, cracking at the strap to DBC interface overwhelms cracking at the die-to-DBC interface. Lastly, the thin solder layer on both sides of the die makes the structure less compliant to induced stresses and strains [109].

Previous studies [111] have subjected the ThinPak^{TM} to –55°C to 125°C temperature cycling with ramp rates of 5°C/min up and 10°C/min down, and a dwell time at the maximum and minimum temperatures of 10 minutes. Early failures revealed weakness in the eutectic solder attachment of the copper strap to the top of the lid. This was due to the large CTE mismatch between the unconstrained copper strap (16 ppm/K) and the underlying alumina ceramic lid (4 ppm/K). These straps were removed and the testing

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continued to the next failure. The second failure occurred at the eutectic solder region where the bottom of the die was attached to the DBC substrate. This interface had a smaller CTE mismatch than the copper strap attachment, with the DBC substrate having a CTE of 10-11 ppm/K, and the silicon die having a CTE of 3 ppm/K. No failures were observed at the high lead solder attach between the alumina ceramic lid (4 ppm/K) and the silicon die (3 ppm/K) either after 2000 thermal cycles or 50,000 power cycles, most likely because of the very close thermal match.

These results show that the double-sided attach approach does have electrical, thermal, and mechanical reliability advantages over a more traditional wirebonding interconnect approach. However, the reliability of the interconnect is STRONGLY dependent on the global CTE mismatch between the surfaces to be joined. Close CTE match between the substrate, lid, and device is necessary, as is the selection of a high temperature solder with good fatigue resistance [109].

Planar Packaging Technology

One of the most recent trends in packaging techniques for power modules is planar packaging, also known as embedded power. In this technique, wire bonds are replaced by direct on-chip interconnections. This eliminates the wire failure mechanisms discussed in the chip and wire modules, and mitigates the attachment fatigue mechanisms critical in the double sided attach module. The use of direct on-chip interconnections leads to very large interfaces between materials. These modules are currently in development by major universities and power electronic system leaders, such as General Electric and Siemens. The layout of materials used is shown in the image below.

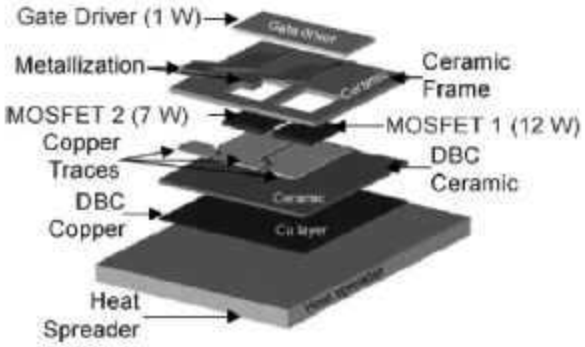

Figure 17 **Structure of an Embedded power device[112]**

This type of module has three major parts. They are the embedded power transistors and diodes, the electronics circuit, and the base substrate. The fabrication process involves embedding dice into a ceramic frame, which is then coated with a dielectric. Currently, this dielectric is a polymer, which limits the maximum use temperature of this type of package to 200°C-250°C. Later, vias are added to provide a direct copper contact to the gate and emitter pads [113]. Connection to the collector is achieved by soldering the part to the metallized base of the ceramic frame. Thus, this module is susceptible to die attach fatigue and substrate fracture as was the case in the chip and wire module and the double

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sided attach module. However, the structure mitigates the stresses causing these failures thereby reducing their occurrence.

Research is needed into new high temperature dielectrics that can be incorporated into planar power modules to create versions that can reliably operate at higher maximum temperatures.

As with the other packaging techniques previously discussed, embedded power also has its own unique set of advantages and disadvantages. First of all, there is a very large contact area, which permits the passage of large currents and good heat transfer. However, this can also lead to additional problems due to the large CTE mismatch between the direct copper interconnects and the underlying devices. Expansion mismatch can cause thermal deformation and delamination of the planar interconnections [112]. One element that helps to counteract these stresses is that the polyimide and epoxy dielectric layers work as stress buffer layers, that absorb stress and improve reliability [114]. Perhaps the greatest advantage of this type of packaging is that the planar structure enables the construction of three-dimensional integrated power electronics systems. A major disadvantage is that little is known about this new technology in terms of failure mechanisms and the actual stress levels in the various embedded layers.

Additional study of the failure mechanisms in planar packaged devices and experimental stress measurements in the embedded layers are in order.

What is known about reliability, however, is that the major issue is the thermomechanical strain between different layers. The top copper layer and the semiconductor device have the highest stresses due to their higher elastic moduli. Thermal and power cycling have been used to test the lifetime and reliability of the modules. An experimental analysis of the reliability of a simplified model, which includes only the polyimide substrate and the copper deposition, has already been completed [114]. The test sample is shown below.

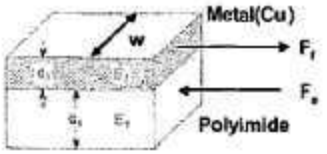

Figure 18 **Simplified model of Embedded power Device [114].**

From this study, it was found that the most common failure modes are yielding of the copper or polyimide, cracking of the copper, and delamination of the copper. This study also showed that 70% of the simplified models failed after only 250 power cycles of ΔT at 80K starting at a base temperature of -10°C, while 10% failed after only 600 temperature cycles between 0°C and 100°C [114].

A similar packaging technique is Planar Power Polymer Packaging, or P4, developed at GE. This technique interconnects power devices with direct metallurgical contacts to the chip pads[115]. Cross-sectional views of the module at various stages of the fabrication process are shown below.

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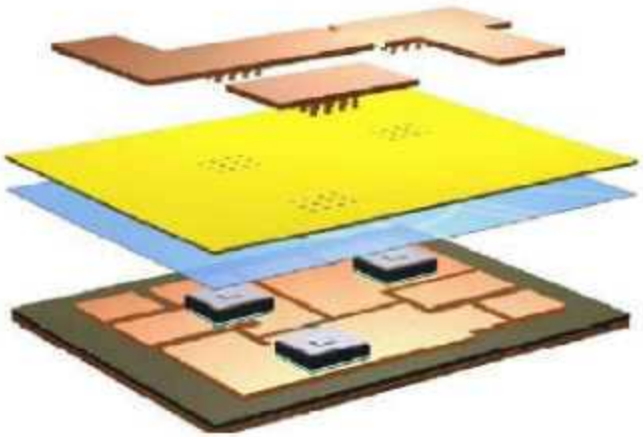

Figure 19 Structure of Planar Power Polymer Packaging device [115]

As with the similar embedded power technique, the P4 packaging technique produces power modules that have a greatly reduced footprint and height, which creates better power density. Also, resistive and inductive interconnect parasitics are reduced by this structure. Lastly, the planar structure eliminates unnecessary structures in the cooling path, which greatly improves the thermal performance of the modules[115]. However, it is susceptible to the same failure mechanisms related to direct copper attach, die attach fatigue, and substrate cracking, and it has the same limitations in use temperature due to the choice of polymer dielectrics. Preliminary reliability studies reveal that the dominant failure mechanism is delamination/cracking of the direct copper attach.

Thus, further reliability analysis of the P4 technology is warranted.

PressPak Technology

A completely different approach to power device packaging is embodied in the IGBT PressPak modules that have been developed in recent years to provide a superior high power alternative to conventional IGBT modules with respect to performance and reliability. A PressPak involves soldering the backside or drain/collector side of silicon transistors and diodes to a metallized ceramic substrate and then interconnecting the top side with a series of springs that apply a constant pressure to obtain good electrical and thermal contact. A PressPak structure eliminates wirebonds, direct copper, and soldered top-side connections and their related failure mechanisms [116]. In order to minimize bowing and shear associated with the thermal mismatch, the PressPak uses sliding contacts, as opposed to a permanent bond such as solder, between the high and low CTE components of the package.

A PressPak power electronic module utilizes compressed springs to connect leads to the IGBT emitter pads and gates. The spring contacting the emitter surface is a bevel spring using inconel washers which are compressed at very high loads in the assembled state (around 500 kN). The inconel washers provide a constant spring constant at high temperatures with little stress relaxation, while signals are shunted around the springs by

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a small copper strap for improved electrical conductivity. The gate contact area on the IGBT chips (around 2.5-mm^2), is a significantly smaller area than the emitter surface (around 100 mm^2) as seen in Figure 20. As a result, a smaller point contact spring is required for contacting the gate. Due to the reduction of surface area contact, a lower loaded spring is required so as to avoid excessive penetration of the gate pad, which can cause a short circuit.

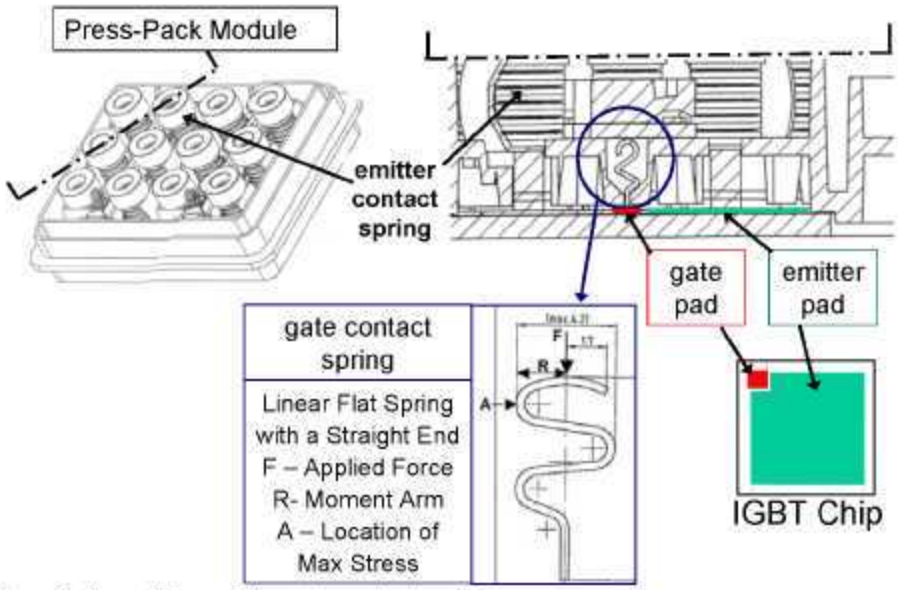

Figure 20 PressPak module and its gate contact spring.

The gate contact spring is typically made of beryllium(2%)-copper C17200 for its good thermal and electrical conductivity and high stiffness properties. BeCu is also known to provide low stress relaxation to temperatures of 175°C – 200°C. Higher use temperatures, up to 300°C-400°C, can be achieved without appreciable stress relaxation by substituting beryllium-nickel. The configuration of the spring is a two dimensional multi-bend configuration known as a flat spring. In order to maintain contact, the spring is initially compressed a fixed displacement when the package is sealed. The point contact at the bottom of the spring must contact the top metallization layer above the gate. However, the spring tip can not be allowed to penetrate to the semiconductor chip. In order to maintain contact and to ensure the operation of the device over its desired lifetime, the gate spring cannot penetrate the metallization layer, and cannot lose contact with the metallization surface during its lifetime. This requires that the chosen initial stress be small enough not to penetrate the metallization layer, but large enough to keep contact with the metallization despite any vibration/shock, or thermal expansion/contraction strains that would act to cause a separation, even when that stress is reduced over time due to stress relaxation at the operating temperature.

The PressPak assembly has additional benefits in very high power applications where high voltage series connections are used. The failure mode of the PressPak IGBT is a short circuit due to the pressure contact structure [117]. This means that if one IGBT

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fails, it will operate in a Short Circuit Failure Mode (SCFM) allowing the system to continue to conduct the total current in the system, requiring replacement only during scheduled maintenance. One method of achieving the SCFM is to metallurgically alloy the silicon with an optimized contact partner. If the partner is chosen properly, a low melting compound is formed leading to a highly conductive path through the chip. This compound will form quickly even at low power. The alloying of the chip occurs immediately after a high current strike causes the metallurgically optimized material to melt and react with the underlying silicon. The result is reliable SCFM performance after device failure [118]. Conventional IGBT modules have a failure mode that is open which prevents the entire system from working in the event of a single IGBT failure. Compression mount devices such as the PressPak have been in use for some time for high power applications because of their superior reliability. Thyristors and GTO thyristors are examples of devices which have been fabricated using a compression mounting assembly.

While PressPaks eliminate the conventional failure mechanisms of wirebond lift-off and mitigate solder fatigue, unsatisfactory mechanical device configurations may lead to unexpected damage and failures. In fact, the non-uniformity of the applied pressure and thermal cycling of materials with high thermal expansion coefficient mismatch can lead to fretting on the gate pads and thermal fatigue of the springs used in the package. Preliminary failure analysis of PressPak devices has confirmed these failure mechanisms [116, 119]. Further research in this area is warranted.

John Hsu Contact Approaches

John Hsu has been examining a contact method that is a variant of the interconnections discussed in the double-sided attach module above. His plans call for the use of one of three types of bonding scenarios. The first is a double-sided soldering approach in which two copper straps are joined with a sintered silver technology to opposite sides of a chip. The use of silver paste instead of eutectic tin-lead solder would make this approach possible at higher temperatures. However, this approach still has the concerns associated with the large CTE mismatch between the copper straps and the silicon die that was mentioned above. As with that attachment, reliability would be improved by keeping the copper strap as thin as possible and ensuring a bend in the copper strap for stress relief. The use of porous and lower modulus silver powder should ameliorate some of the concern, as it has been shown that sintered silver flake manufactured using the 40 MPa pressure approach has a much longer life than eutectic solder in a fixed application, but it would still be necessary to conduct modeling and accelerated testing to establish that the technique would provide sufficient reliability for this intended application. Such testing would include thermal cycling while monitoring forward voltage.

The second approach is similar to the first, but includes the division of the copper strap into a series of copper fingers. This approach will have improved reliability over the first approach because it limits the strain field generated by the CTE mismatch with no appreciable downside, except for some localization of current and some reduction in heat

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transfer, neither of which should significantly impact the reliability. The number of fingers should be large enough to reduce the strain field, but not so large as to induce current crowding and distribution effects. Three to eight fingers is usually optimal. Furthermore, it would be a good idea to run a conduction thermal analysis to determine the change in ΔT that occurs during power on/off cycles as a result of the smaller heat transfer surface.

The third approach is a variation on the second approach, but it includes a spacer to limit the susceptibility of the joint to failure by shock and vibration. While the spacer would limit the potential displacement and curvature of the copper strap during vibration loading, it would be useful to conduct a vibration analysis to determine the maximum expected displacement in the fundamental mode to see if use of the spacer is needed. Furthermore, it is important that the spacer be of a ceramic that is thermally matched to the silicon, so that it does not cause expansion related peeling stresses on the copper strap during thermal excursions.

John Hsu is also investigating the effect of placing wirebonds, copper straps, or similar interconnects into a boiling cooling fluid. Wirebonds or similar interconnections exposed to the agitation of a boiling fluid would be subjected to a number of stresses. First, at the initiation of boiling, small bubbles would form and then rapidly collapse. Each time a bubble collapsed, it would send a shock wave through the fluid. These shock waves can be quite sizeable in force and could cause vibration of the wirebonds. Second, as boiling proceeded, the circulation of the fluid could cause wire sweep and lateral motion of the wirebonds, which would be a function of the viscosity of the fluid. Fluorinert, or other insulating fluorocarbon liquids, have viscosities (1.4 cP) on the order of water and should be somewhat benign in this respect. The wires, however, should be spaced well apart in order to ensure that they do not brush against one another in the swirling liquid which, if it occurred, would cause intermittent shorting. Copper straps, and thicker (5-15 mil), wedge bonded aluminum wires such as are typical in power electronics, would be more immune to all these forces than thinner (0.8-1.2 mil), ball bonded gold wires. In fact, it is quite common in thermal management and cooling experiments to place exposed thick wirebonds directly in the cooling fluid. At least in the short run and from the standpoint of overstressing the wires, this does not appear to generate any practical concern. The location on the chip where the boiling is occurring is far enough away from the wirebonds to minimize the stress, and no overstress failures of the wirebonds have been observed. The long term reliability effects of fatigue due to small lateral motions of the wires has not yet been investigated, but, it appears from these initial studies, that wirebonds are able to withstand the boiling with minimal damage. This is much different from the case of ultrasonic agitation of very thin gold bond wires in which the wirebonds effectively couple the high frequency vibration energy and fail rapidly.

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Summary and Conclusions

Technology related to the development of electronics that can operate in the high temperature environments present in hybrid vehicles has been advancing rapidly. The latest technology developments, commercially available components, and packaging approaches have been detailed in this report. Each of these elements has advantages and disadvantages that must be traded off in order to design an optimum high temperature electronic system containing both small signal control and power electronic devices. Furthermore, each element is susceptible to different failure mechanisms that must be mitigated to provide reliable long term operation. Where the commercially available elements were not up to the challenge of long term operation in the hybrid vehicle environment, alternative designs were suggested or further research was recommended.

Collected Suggestions for Further Research

- Develop specific mission profiles and accelerated testing protocols for the underhood environment for hybrid cars, as has previously been done for gasoline-powered vehicles.
- Further effort in the development of SiC MOSFETs and IGBTs and their associated packaging.
- Address limitations to SiC power devices, including screw dislocation assisted reverse breakdown, ohmic contact issues, interconnection and packaging.
- Address the resistance of the gold-based metallizations to electromigration
- Model fatigue of aluminum wirebonds to improve power electronic module reliability.
- Model copper wire-copper bondpad liftoff failures as power devices move to copper metallization.
- Model the reliability of sintered silver nanopowders and develop alternative high temperature solder/attach techniques.
- Develop silicon nitride substrate technology, especially metallization.
- Develop new high temperature dielectrics that can be incorporated into planar power modules to create version that can reliably operate at higher maximum temperatures.
- Investigate failure mechanisms in planar packaged devices and conduct experimental stress measurements in the embedded layers of P4.

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